

TL0301H: 4.9 – 6.0 GHz High Gain Ultra Low Noise Amplifier

1.0 Features

- Small signal gain @ 5.5 GHz: 17.8 dB
- EVB NF @ 5.5 GHz: 1 dB
- IP1dB @ 5.5 GHz: -4.5 dBm
- 3.3V Typical operating voltage
- Operating frequency: 4.9 to 6.0 GHz



Figure 1.1 Device Image
(6 Pin 1.5×1.5×0.8mm DFN Package)

2.0 Applications

- IEEE 802.11 b/g/a/n/ac Wi-Fi, WLAN
- Small Cells and Cellular Repeaters
- 4G Infrastructure Radios
- Phase Array Radar



**RoHS/REACH/Halogen Free
Compliance**

3.0 Description

The TL0301H is a High Gain, Ultra-low Noise Amplifier (LNA) providing high gain and linearity. Over the above-mentioned frequency band, this device exhibits excellent noise figure of 1.0 dB (SMA-SMA) with outstanding gain flatness.

The LNA is operated with a typical bias condition of 3.3 V and 15 mA. TL0301H is internally matched to 50 Ω at the input and output ports.

The TL0301H is packaged in a compact, low-cost DFN 1.5x1.5x0.8mm, 6 pin plastic package.

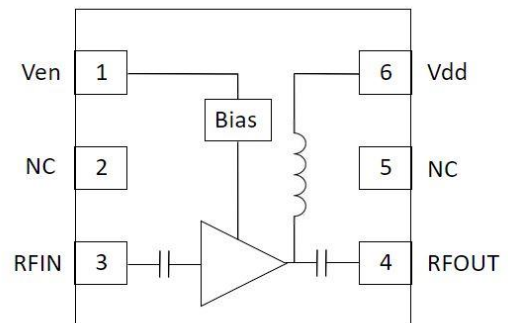


Figure 3.1 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 4.1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TL0301H	Pin 1.5×1.5×0.8mm DFN	Tape and Reel	5000	13" (330mm)	18mm	TL0301HMTRPBF
Tuned Evaluation Board, 5.125-5.925GHz						TL0301H-EVB-A

5.0 Pin Description

Table 5.1 Pin Definition

Pin Number	Pin Name	Description
1	Ven	Venable along with series resistor sets the Idq. Venable <0.2V disables the device
2	NC	No internal connection, can be connected to ground
3	RFIN	RF Input. DC blocking cap required
4	RFOUT	RF Output
5	NC	No internal connection, can be connected to ground
6	V _{dd}	Supply Voltage for the LNA, supplied through an external choke inductor
Package Base	Paddle/Slug	DC and RF Ground. Also provides thermal relief. Multiple vias are recommended

Note: [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heat sinking required.

6.0 Absolute Maximum Rating

Table 6.1 Absolute Maximum Rating @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Supply voltage, Venable	V _{dd} , Ven	+6	V
Drain current	I _{DQ}	25	mA
RF input power CW	RFIN	15	dBm
Storage Temperature Range	T _{st}	-55 to +150	°C
Operating Temperature Range	T _{op}	-40 to +105	°C
Maximum Junction Temperature	T _J	170	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	R _{θJC}	15.0	°C/W
Soldering Temperature	T _{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention: Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Recommended DC Operating Conditions

Table 7.1 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltage	V_{DD}		+3.3		V
Venable Voltage	V_{en}		+3.3		V
Drain Bias Current	I_{DQ} , Set by external resistor		15.0		mA
Venable Bias Current	I_{bias}		2.0		mA
Operating Temperature Range		-40	+25	+105	°C

8.0 RF Electrical Specifications for 5.1-5.925 GHz EVB

Table 8.1 5.1-5.925 GHz EVB @ $T_A=+25^\circ\text{C}$ Unless Otherwise Specified; $V_{en}=V_{dd}=3.3\text{V}$, $I_{dd}=15\text{mA}$

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across the band		16-18		dB
Noise Figure	Across the band		0.8-1.1		dB
EVB Noise Figure	Across the band		0.9-1.2		dB
Input Return Loss	Across the band		9-10		dB
Output Return Loss	Across the band		5-7		dB
IP1dB	Across the band		-3 to -5		dBm
IIP3	Across the band, 0dBm per tone, Tone Spacing 1MHz		0-1.1		dBm

9.0 Typical Characteristics

9.1 5.125GHz – 5.925GHz tuned EVB (Vdd=3.3V, IdQ=15mA) @ TA=+25°C



Figure 9.1 S21(Gain) vs Freq

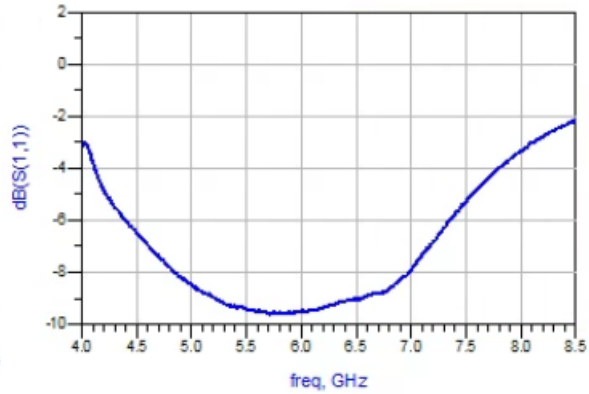


Figure 9.2 S11 (IRL) vs Freq

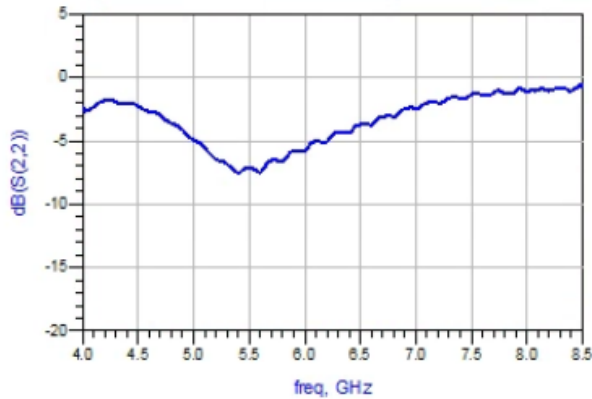


Figure 9.3 S22 (ORL) vs Freq

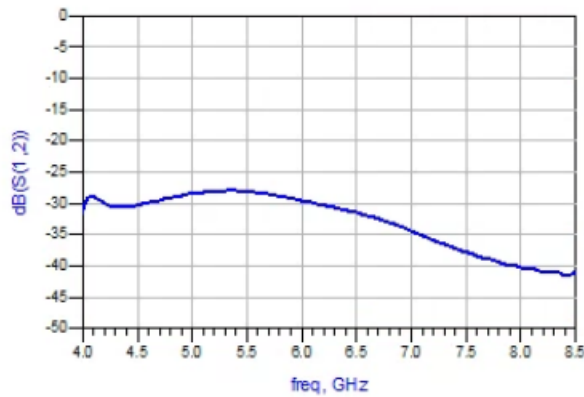


Figure 9.4 S12(Reverse Isolation) vs Freq

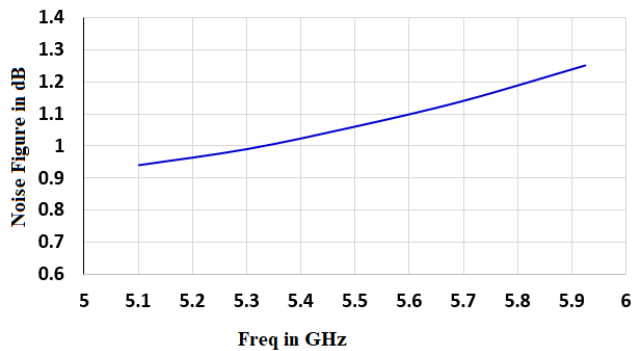


Figure 9.5 EVB Noise Figure vs Freq

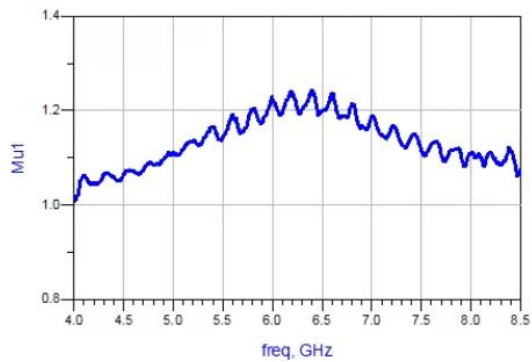


Figure 9.6 Stability (Mu1) vs Freq

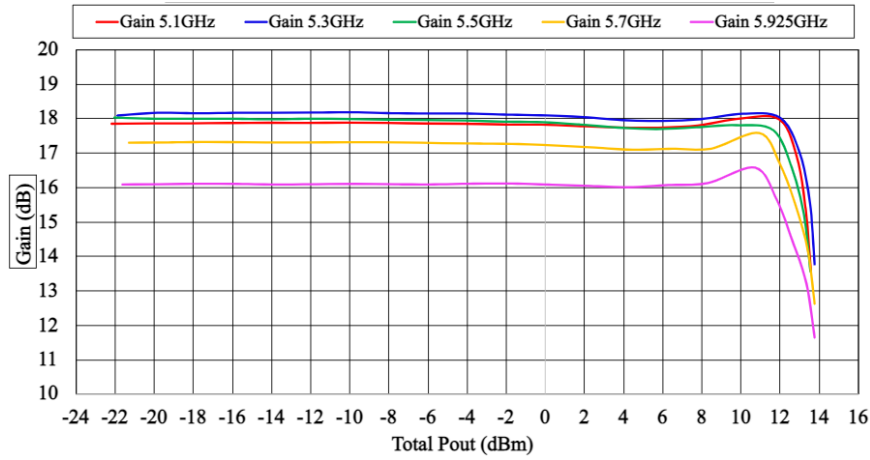


Figure 9.7 Output P1dB vs Pout for all Freq

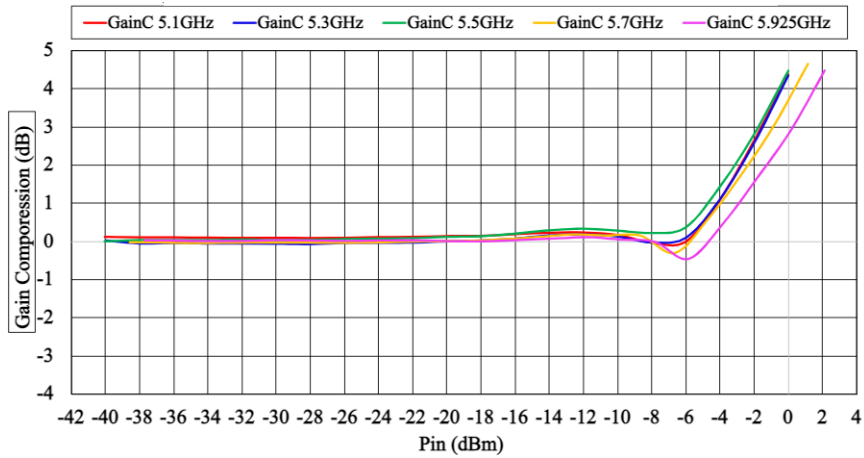


Figure 9.8 Gain compression Vs Pin for all Freq

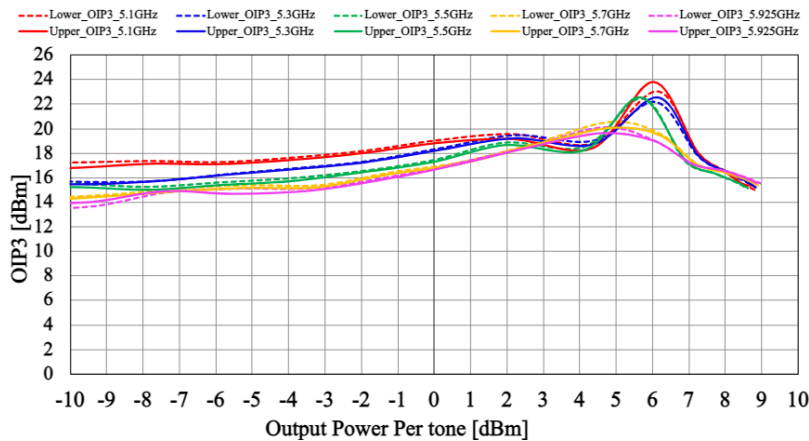


Figure 9.9 OIP3 vs Pout per tone for all Freq

10.0 Evaluation Boards

10.1 5.1-5.925 GHz EVB (V_{dd}=3.3V, I_{bq}=15mA)

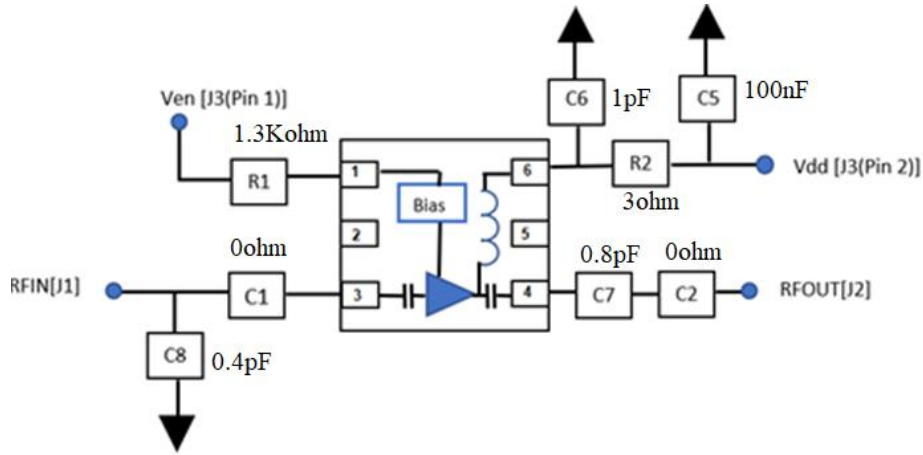


Figure 10.1 Schematic of the 5.1-5.925 GHz EVB

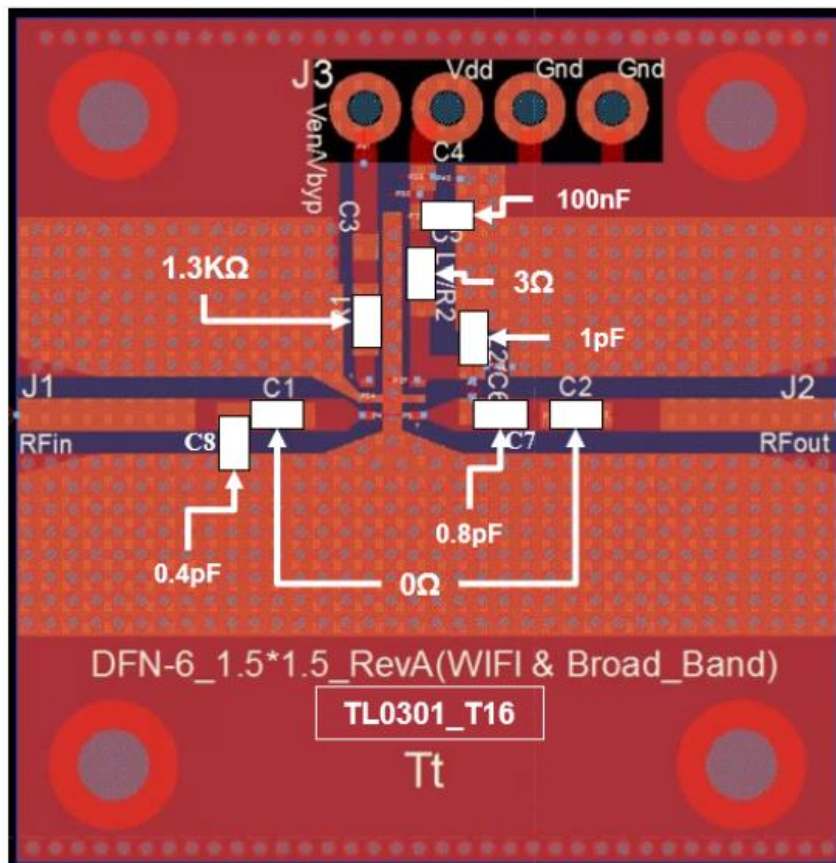


Figure 10.2 Board Layout of the 5.1-5.925 GHz EVB

Table 10.1 BOM of the 5.1-5.925 GHz EVB

Component ID	Value	Manufacturer	Recommended Part Number
C1, C2	0Ω	Panasonic	ERJ-2GE0R00X
R1	1.3KΩ	Panasonic	ERJ-2RKF1301X
R2	3Ω	Vishay	CRCW06033R00FKEAHP
C5	100nF	TDK	C1005X7R1H104K050BE
C6	1pF	Murata	GJM1555C1H1R0BB01D
C7	0.8 pF	Murata	GJM1555C1HR80BB01D
C8	0.4 pF	Murata	GJM1555C1HR40BB01D
PCB	Rogers RO4350B, 20 mils, 1 oz Copper		

11.0 Device Package Information

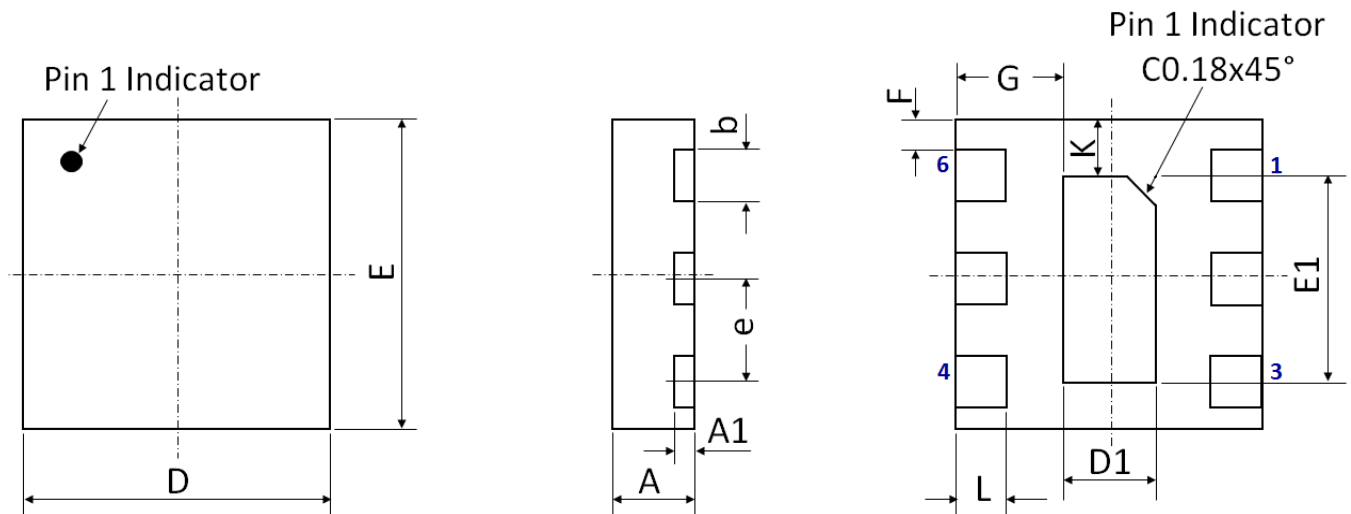


Figure 11.1 Device Package Drawing
(All dimensions are in mm)

Table 11.1 Device Package Dimensions

Dimension (mm)	Value (mm)	Tolerance(mm)	Dimension (mm)	Value (mm)	Tolerance(mm)
A	0.55	±0.05	E	1.50 BSC	±0.05
A1	0.15	±0.02	E1	1.00	±0.05
b	0.25	±0.02	F	0.15	±0.02
D	1.50 BSC	±0.05	G	0.525	±0.05
D1	0.45	±0.02	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.28	±0.02

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention: Please refer to application notes *TN-001* and *TN-002* at <http://www.tagoretech.com> for PCB and soldering related guidelines.

12.0 PCB Land Design

Guidelines:

- [1] 4-layer PCB is recommended
- [2] Via diameter is recommended to be 0.3mm for better thermal performance
- [3] Thermal vias shall be placed on the center pad and should be filled/plugged with solder or copper
- [4] The maximum via number for the center pad is $1(X) \times 2(Y) = 2$

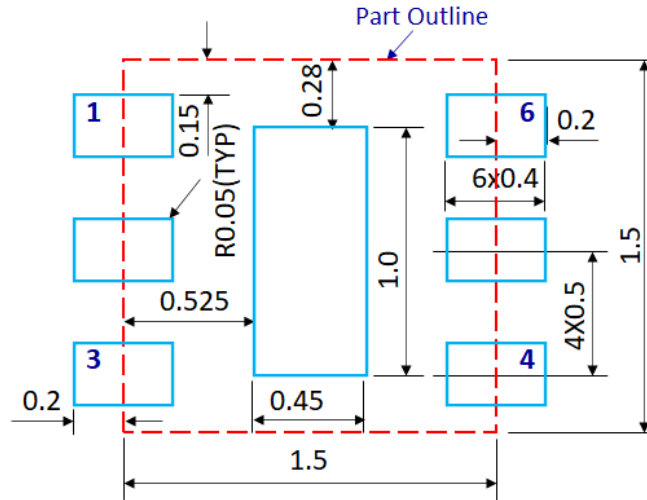


Figure 12.1 PCB Land Pattern
(Dimensions are in mm)

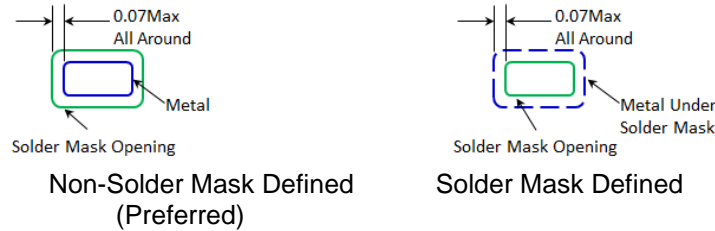


Figure 12.2 Solder Mask Pattern
(Dimensions are in mm)

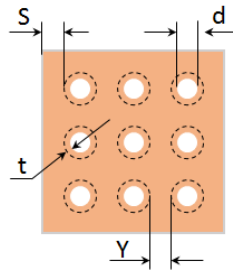


Figure 12.3 Thermal Via Pattern

(Recommended Values: $S \geq 0.15\text{mm}$; $Y \geq 0.20\text{mm}$; $d = 0.3\text{mm}$; Plating Thickness $t = 25\mu\text{m}$ or $50\mu\text{m}$)

13.0 PCB Stencil Design

Guidelines:

- [1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- [2] Stencil thickness is recommended to be 125µm.

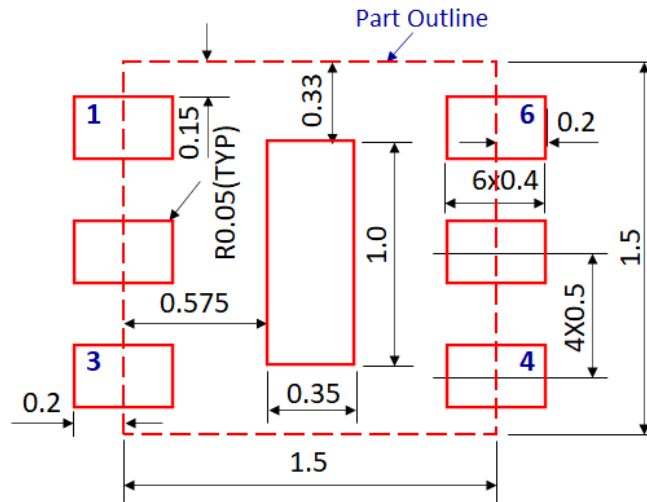


Figure 13.1 Stencil Openings
(Dimensions are in mm)

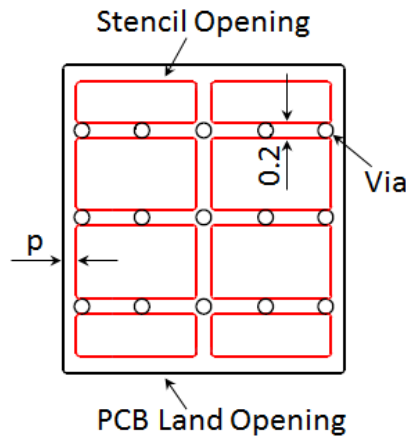


Figure 13.2 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

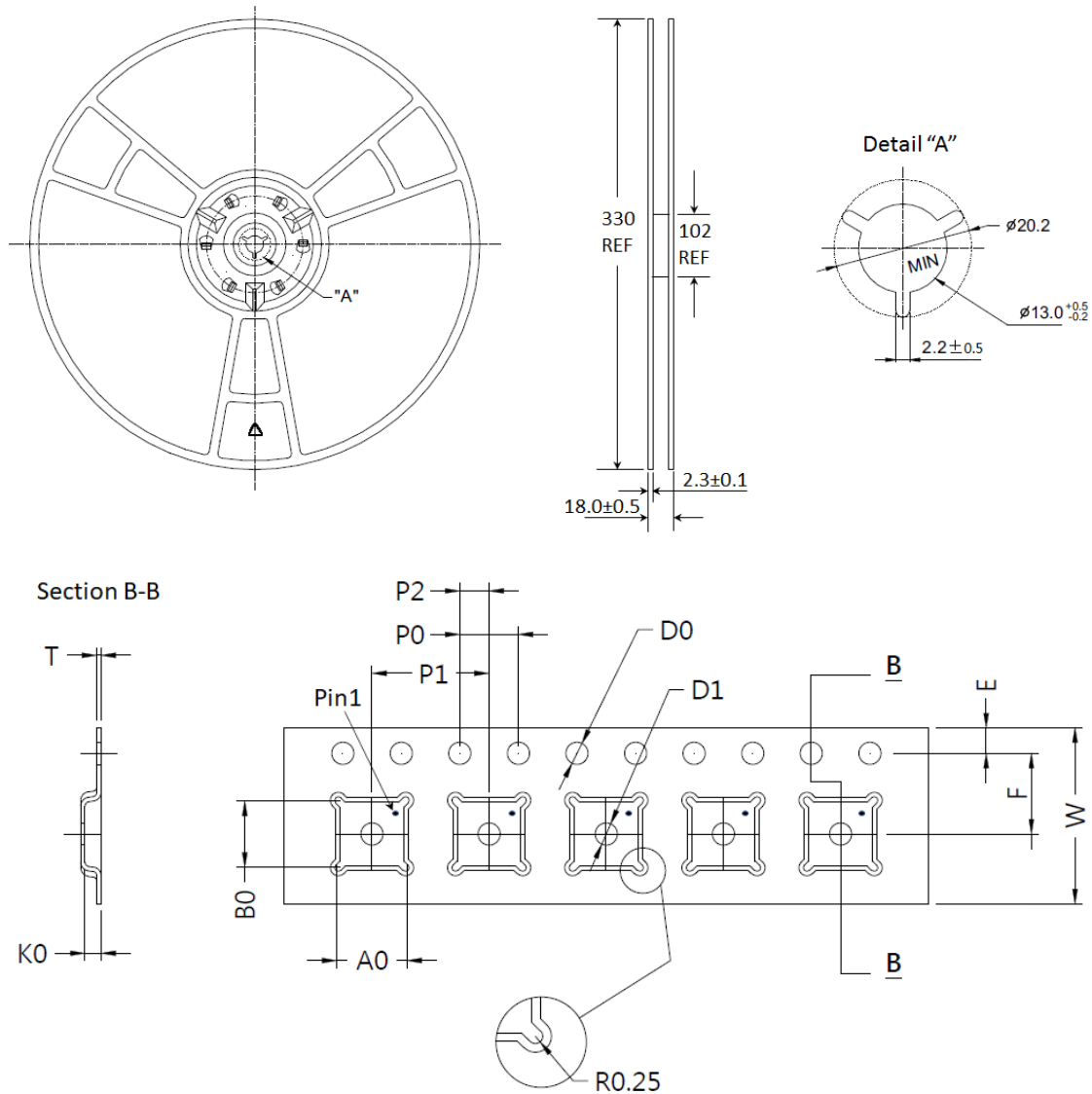


Figure 14.1 Tape and Reel Drawing

Table 14.1 Tape and Reel Dimensions

Dimension (mm)	Value (mm)	Tolerance(mm)	Dimension (mm)	Value (mm)	Tolerance(mm)
A0	3.35	±0.10	K0	1.10	±0.10
B0	3.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

Edition Revision 1.3 - 2022-10-31

Published by

Tagore Technology Inc.
601 W Campus Dr. Ste C1
Arlington Heights, IL 60004, USA

©2022 All Rights Reserved

Legal Disclaimer

The information provided in this document shall in no event be regarded as a guarantee of conditions or characteristics. Tagore Technology assumes no responsibility for the consequences of the use of this information, nor for any infringement of patents or of other rights of third parties which may result from the use of this information. No license is granted by implication or otherwise under any patent or patent rights of Tagore Technology. The specifications mentioned in this document are subject to change without notice.

Information

For further information on technology, delivery terms and conditions and prices, please contact Tagore Technology: support@tagoretech.com.