

## TL0375J: 2.0 – 5.0 GHz GaAs Ultra Low Noise Amplifier

### 1.0 Features

- Small signal gain @ 3600MHz: 17.5dB
- NF @ 3600MHz: 0.4dB
- OP1dB @ 3600MHz: 19.5dBm
- OIP3dB @ 3600MHz: 32.5dBm
- 5V Typical operating voltage
- Operating frequency: 2.0 to 5.0GHz



**Figure 1.1 Device Image**  
(8 Pin 2x2x0.75mm QFN Package)

### 2.0 Applications

- 4G/5G Infrastructure Radios
- Small Cells and Cellular Repeaters
- Phase Array Radar
- SDARS

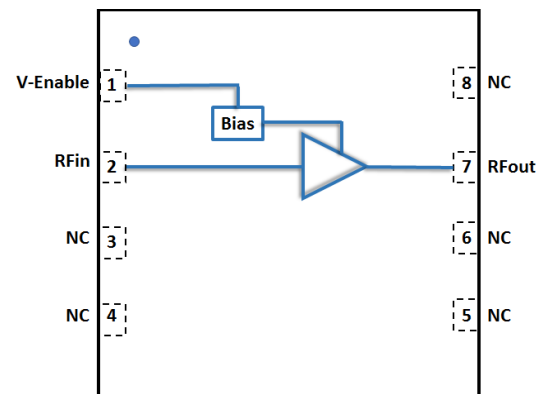


**RoHS/REACH/Halogen Free Compliance**

### 3.0 Description

The TL0375J is a high frequency version of TL0374J which is a broadband, ultra-low Noise Amplifier (LNA). With a simple input and output match, this LNA can be tuned for different frequency bands targeting LTE (small cells and infrastructure), radar and any other applications requiring low noise, high gain, and linearity.

The TL0375J is packaged in a compact, low-cost Dual Flat No Lead (DFN) 2x2x0.75mm, 8 pin plastic package.



**Figure 3.1 Function Block Diagram**  
(Top View)

### 4.0 Ordering Information

**Table 4.1 Ordering Information**

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TL0375J	8 Pin 2x2x0.75mm DFN	Tape and Reel	5000	13" (330mm)	18mm	TL0375JMTRPBF
Tuned Evaluation Board, 3300 - 3800MHz						TL0375J-EVB-A
Tuned Evaluation Board, 3700 - 4200MHz						TL0375J-EVB-B
Tuned Evaluation Board, 4400 - 5000MHz						TL0375J-EVB-C
Tuned Evaluation Board, 2900 - 3300MHz						TL0375J-EVB-D

## 5.0 Pin Description

**Table 5.1 Pin Definition**

Pin Number	Pin Name	Description
3-6, 8	NC	No internal connection, can be connected to ground
1	Venable	Venable along with series resistor, sets the Idq. Venable <0.2V disables the device
2	RF <sub>IN</sub>	RF Input. DC blocking cap required
7	RF <sub>OUT</sub> /V <sub>dd</sub>	RF Output. Vdd supplied through an external choke inductor
Package Base	Paddle/Slug	DC and RF Ground. Also provides thermal relief. Multiple vias are recommended

**Note:** [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heatsinking required.

## 6.0 Absolute Maximum Rating

**Table 6.1 Absolute Maximum Rating @T<sub>A</sub>=+25°C Unless Otherwise Specified**

Parameter	Symbol	Value	Unit
<b>Electrical Ratings</b>			
Supply voltage, Venable	V <sub>dd</sub>	+6	V
Drain current	I <sub>DQ</sub>	70	mA
RF input power CW	RF <sub>IN</sub>	23	dBm
Storage Temperature Range	T <sub>st</sub>	-55 to +150	°C
Operating Temperature Range	T <sub>op</sub>	-40 to +105	°C
Maximum Junction Temperature	T <sub>J</sub>	170	°C
<b>Thermal Ratings</b>			
Thermal Resistance (junction-to-case) – Bottom side	R <sub>θJC</sub>	15.0	°C/W
Soldering Temperature	T <sub>SOLD</sub>	260	°C
<b>ESD Ratings</b>			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C	≥1000	V
<b>Moisture Rating</b>			
Moisture Sensitivity Level	MSL	1	-

### Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

## 7.0 Recommended DC Operating Conditions

**Table 7.1 Recommended Operating Conditions**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltage	$V_{DD}$		+5.0		V
Venable Voltage	$V_{enable}$		+5.0		V
Drain Bias Current	$I_{DQ}$ , Set by external resistor	45	60		mA
Venable Bias Current	$I_{bias}$		3.0		mA
Operating Temperature Range		-40	+25	+105	°C

## 8.0 Switching Time

**Table 8.1 Switching time.**

Parameter	Test Condition	Typical	Unit
Switching Rise Time	10/90% of the RF value	300	nsec
Switching Fall Time	10/90% of the RF value	350	nsec

## 9.0 RF Electrical Specifications

**Table 9.1 EVB A 3300-3800MHz**

Venable= 5V, Idd=60mA, Vdd=5V, @TA=+25°C Unless Otherwise Specified

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across Band		17.4-18.2		dB
Noise Figure	Across Band		0.45-0.55		dB
EVB Noise Figure	Across Band		0.5-0.6		dB
Input Return Loss	Across Band		15-16		dB
Output Return Loss	Across Band		8.4-10.6		dB
OP1dB	Across Band		19.3-20		dBm
OIP3	Across Band ,0dBm per tone, Tone Spacing 1MHz		32.5-33.5		dBm

**Table 9.2 EVB B 3700-4200MHz**

Venable= 5V, Idd=60mA, Vdd=5V, @TA=+25°C Unless Otherwise Specified

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across Band		15.5-16.5		dB
Noise Figure	Across Band		0.5-0.6		dB
EVB Noise Figure	Across Band		0.6-0.7		dB
Input Return Loss	Across Band		8-12		dB
Output Return Loss	Across Band		8-12		dB
OP1dB	Across Band		19-20.5		dBm
OIP3	Across Band, 0dBm per tone, Tone Spacing 1MHz		33-34		dBm

**Table 9.3 EVB C 4400-5000MHz**

Venable= 5V, Idd=60mA, Vdd=5V, @TA=+25°C Unless Otherwise Specified

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across Band		16		dB
Noise Figure	Across Band		0.55-0.65		dB
EVB Noise Figure	Across Band		0.7-0.8		dB
Input Return Loss	Across Band		10.4-12.4		dB
Output Return Loss	Across Band		7.5-9		dB
OP1dB	Across Band		18-20		dBm
OIP3	Across Band, 0dBm per tone, Tone Spacing 1MHz		33-36		dBm

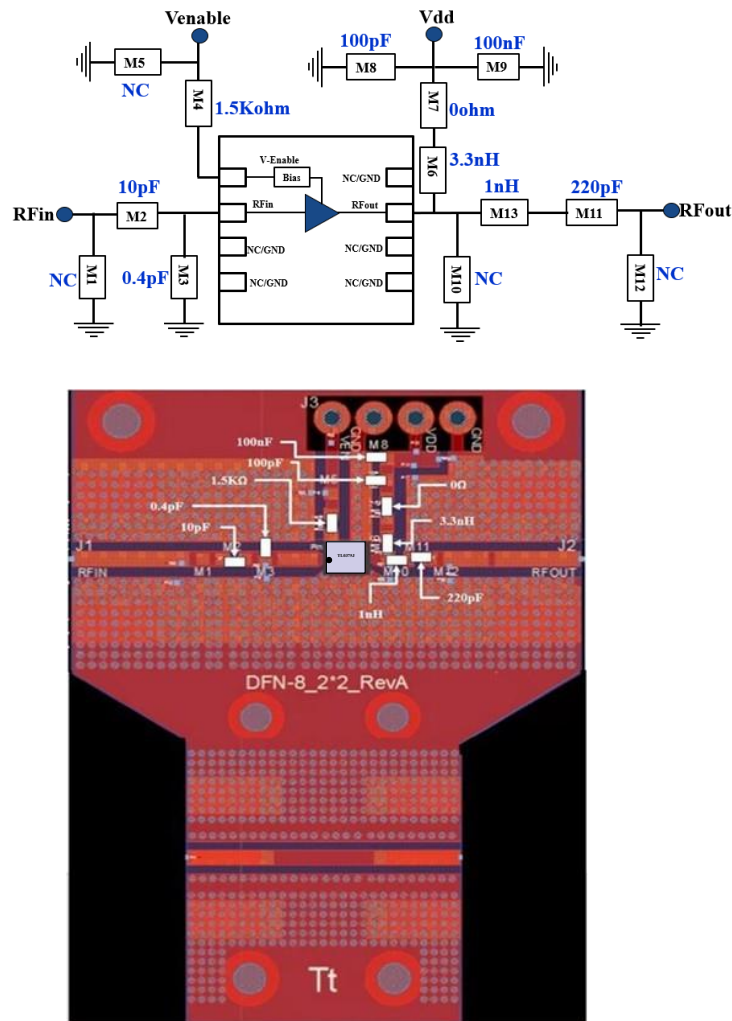
**Table 9.4 EVB D 2900-3300MHz**

Venable= 5V, Idd=65mA, Vdd=5V, @TA=+25°C Unless Otherwise Specified

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across Band		18.5-17.9		dB
Noise Figure	Across Band		0.35-0.45		dB
EVB Noise Figure	Across Band		0.4-0.5		dB
Input Return Loss	Across Band		19-13		dB
Output Return Loss	Across Band		8.3-6		dB
OP1dB	Across Band		19.3-19.4		dBm
OIP3	Across Band, 0dBm per tone, Tone Spacing 1MHz		33.8-35.5		dBm

## 10.0 Evaluation Board Details

### 10.1 EVB A 3.3-3.8GHz

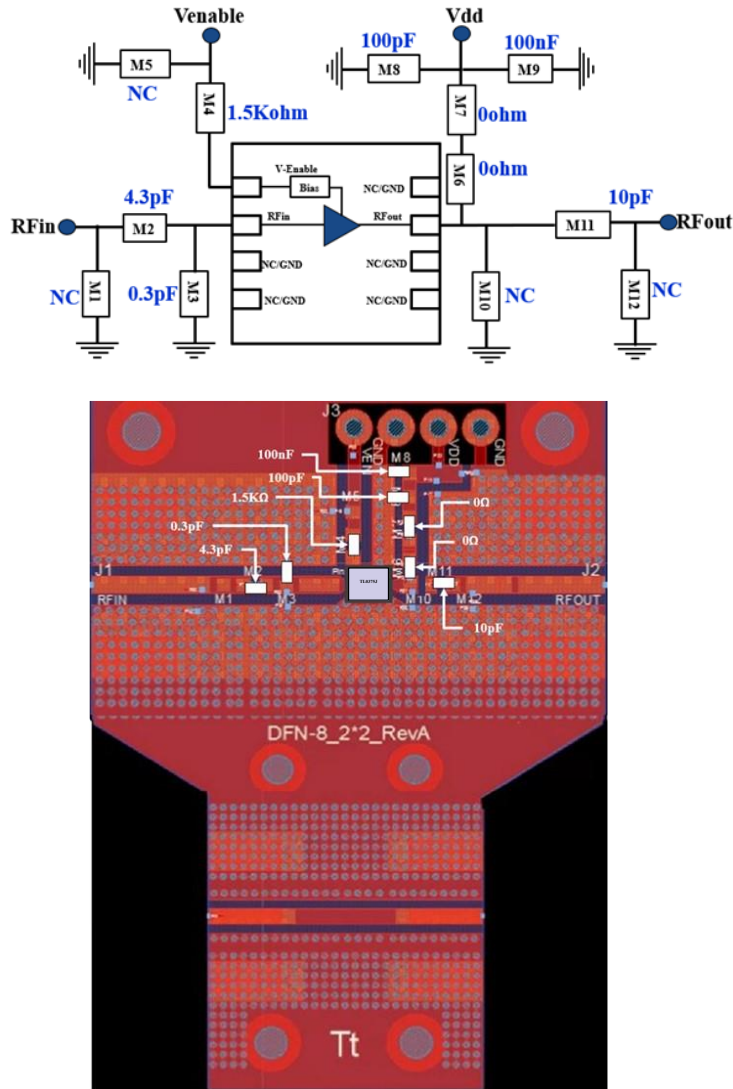


**Figure 10.1 Schematic and EVB layout of the 3300-3800MHz EVB-A**

**Table 10.1 BOM of the 3300-3800MHz EVB A**

Component ID	Value	Manufacturer	Recommended Part Number
M2	10pF	Murata	GJM1555C1H100JB01
M3	0.4pF	Murata	GJM1555C1HR40BB01
M6	3.3nH	Coil craft	0402HP-3N3XGE
M4	1.5KΩ	Panasonic	ERJ-2RKF1501X
M8	100pF	AVX	04025A101JAT4A
M9	100nF	TDK	C1005X7R1H104K050BE
M7	0Ω	Panasonic	ERJ-2GE0R00X
M11	220pF	Kemet	C0402C221K5GACAUTO
M13	1nH	coil craft	0402HP-1N0XJE
PCB		Rogers RO4350B, 20 mils, 1 oz copper	

**10.2 EVB B 3.7-4.2GHz**

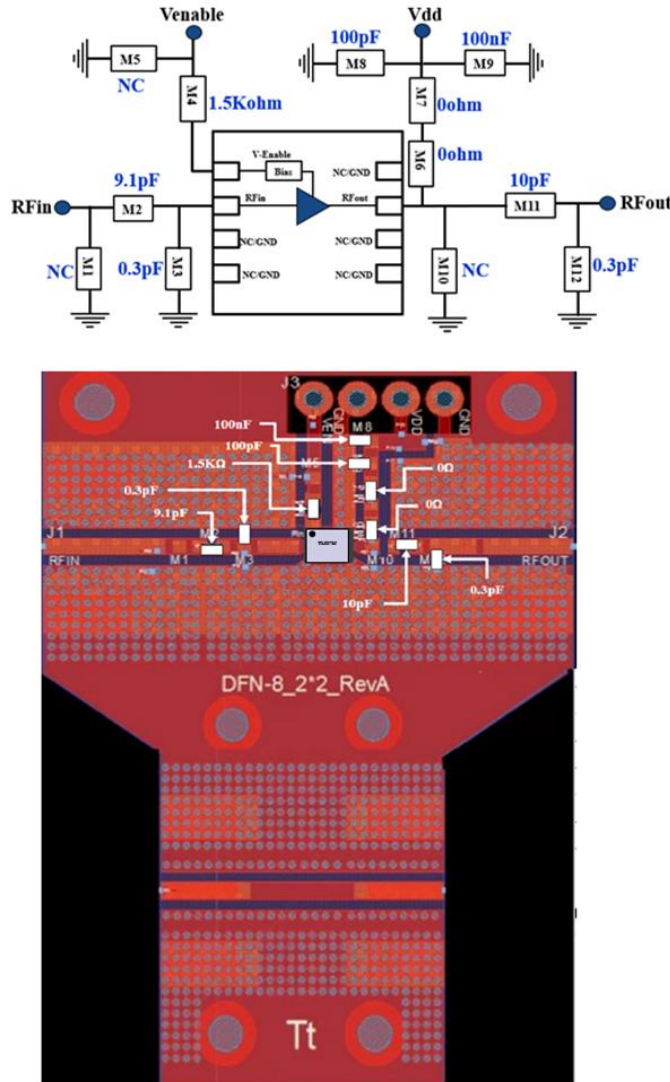


**Figure 10.2 Schematic and EVB layout of the 3700-4200MHz EVB-B**

**Table 10.2 BOM of the 3700-4200MHz EVB B**

Component ID	Value	Manufacturer	Recommended Part Number
M2	4.3pF	Murata	GJM1555C1H4R3BB01
M3	0.3pF	Murata	GJM1555C1HR30BB01
M4	1.5KΩ	Panasonic	ERJ-2RKF1501X
M8	100pF	AVX	04025A101JAT4A
M9	100nF	TDK	C1005X7R1H104K050BE
M6, M7	0Ω	Panasonic	ERJ-2GE0R00X
M11	10pF	AVX	04025A100JAT4A
Q1	GaAs LNA	Tagore Technology	TL0375J
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

**10.3 EVB C 4.4-5.0GHz**



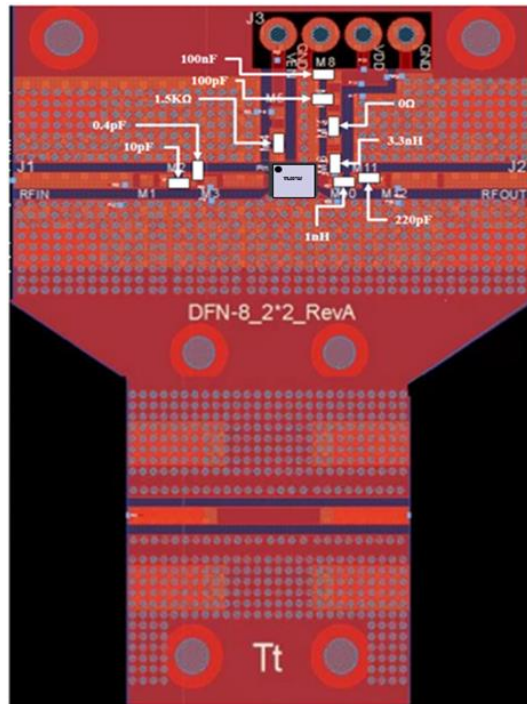
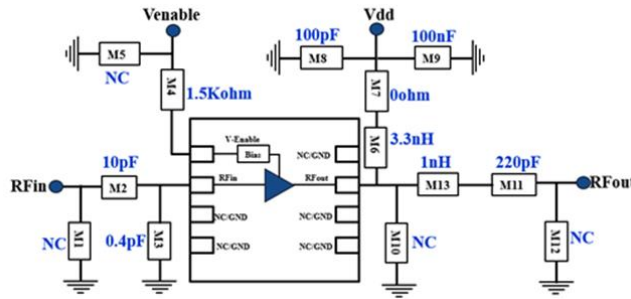
**Figure 10.3 Schematic and EVB layout of the 4400-5000MHz EVB-C**

**Table 10.3 BOM of the 4400-5000MHz EVB C**

Component ID	Value	Manufacturer	Recommended Part Number
M2	9.1pF	Murata	GJM1555C1H9R1BB01
M4	1.5KΩ	Panasonic	ERJ-2RKF1501X
M3	0.3pF	Murata	GJM1555C1HR30BB01
M8	100pF	AVX	04025A101JAT4A
M9	100nF	TDK	C1005X7R1H104K050BE
M6,M7	0Ω	Panasonic	ERJ-2GE0R00X
M11	10pF	AVX	04025A100JAT4A
M12	0.3pF	Murata	GJM1555C1HR30BB01
Q1	GaAs LNA	Tagore Technology	TL0375J
PCB	Rogers RO4350B, 20 mils, 1 oz copper		



**10.4 EVB D 2.9-3.3GHz**



**Figure 10.4 Schematic and EVB layout of the 2900-3300MHz EVB-D**

**Table 10.4 BOM of the 2900-3300MHz EVB D**

Component ID	Value	Manufacturer	Recommended Part Number
M2	10pF	Murata	GJM1555C1H100JB01
M3	0.4pF	Murata	GJM1555C1HR40BB01
M6	3.3nH	Coil craft / Wurth Electronics	0402HP-3N3XGE / 744916033
M4	1.5KΩ	Panasonic	ERJ-2RKF1501X
M8	100pF	AVX	04025A101JAT4A
M9	100nF	TDK	C1005X7R1H104K050BE
M7	0Ω	Panasonic	ERJ-2GE0R00X
M11	220pF	Kemet	C0402C221K5GACAUTO
M13	1nH	Coil craft / Wurth Electronics	0402HP-1N0XJE / 744916010
Q1	GaAs LNA	Tagore Technology	TL0375J
PCB	Rogers RO4350B, 20 mils, 1 oz copper		



## 11.0 Typical Characteristics

### 11.1 3300 - 3800MHz tuned EVB (V<sub>dd</sub>=5V, I<sub>DQ</sub>=60mA), -40°C, 25°C, 85°C, 105 °C, Narrowband

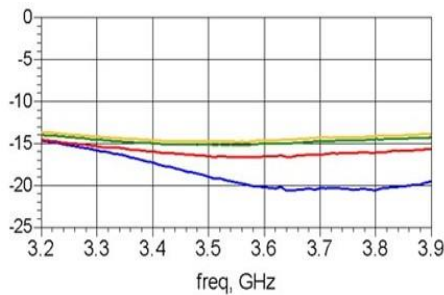


Figure 11.1.1: S11(IRL) vs Freq

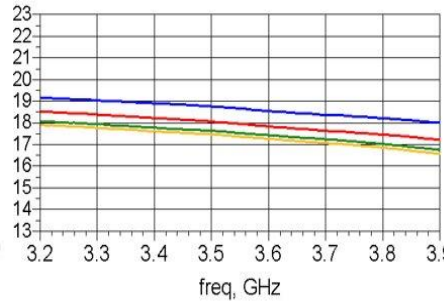


Figure 11.1.2: S21(Gain) vs Freq

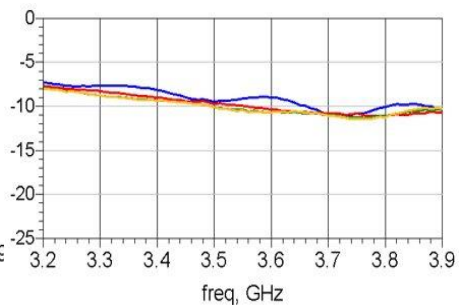


Figure 11.1.3: S12(Rev Iso) vs Freq

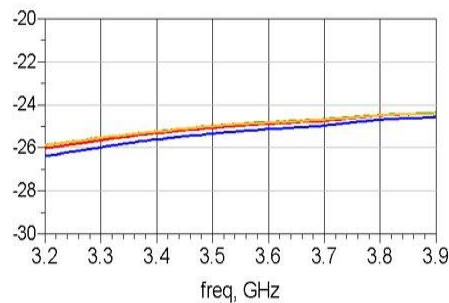


Figure 11.1.4: S22(ORL) vs Freq

### 11.2 3300 - 3800MHz tuned EVB (V<sub>dd</sub>=5V, I<sub>DQ</sub>=60mA), -40°C, 25°C, 85°C, 105 °C, Broadband

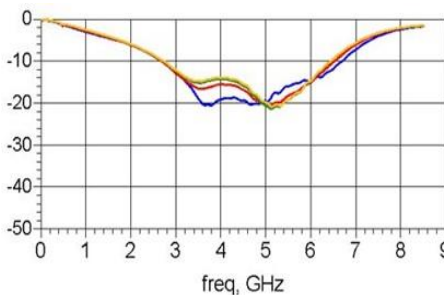


Figure 11.2.1: S11(IRL) vs Freq

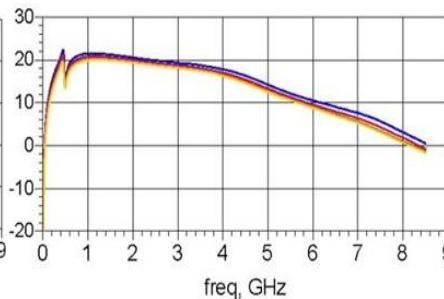


Figure 11.2.2: S21(Gain) vs Freq

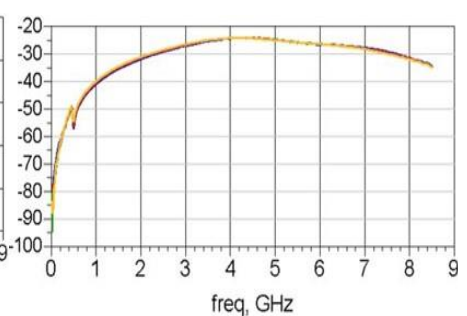


Figure 11.2.3: S12(Rev Iso) vs Freq

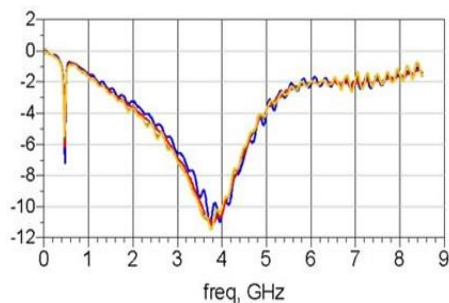
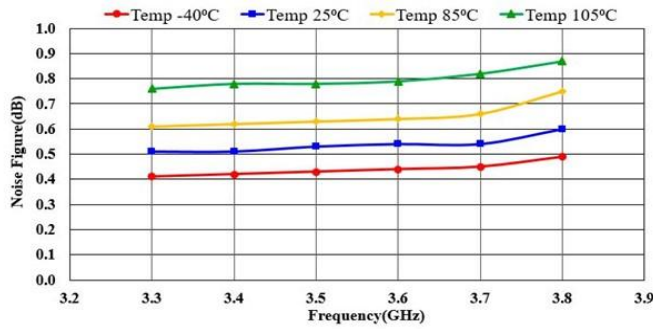
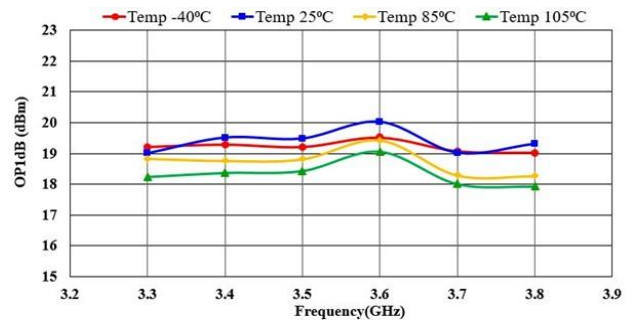


Figure 11.2.4: S22(ORL) vs Freq

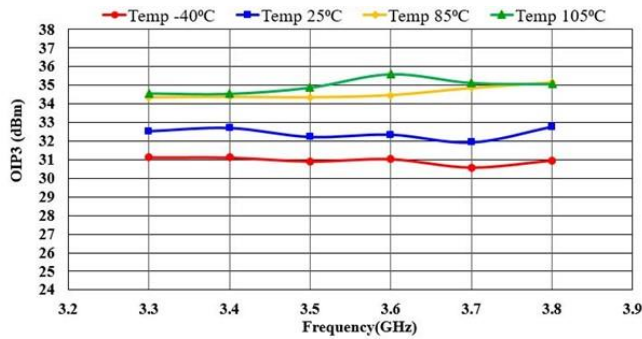
**11.3 3300 - 3800MHz tuned EVB (Vdd=5V, I<sub>DQ</sub>=60mA), -40°C, 25°C, 85°C, 105 °C, Large Signal Data**



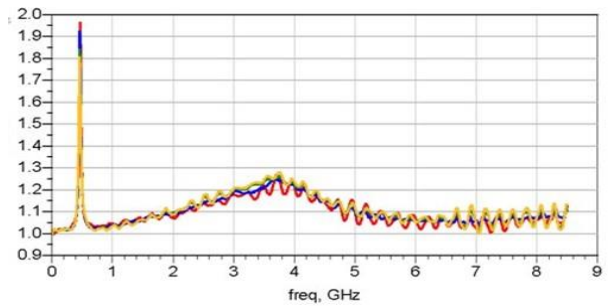
**Figure 11.3.1: Noise Figure (EVB) vs Freq**



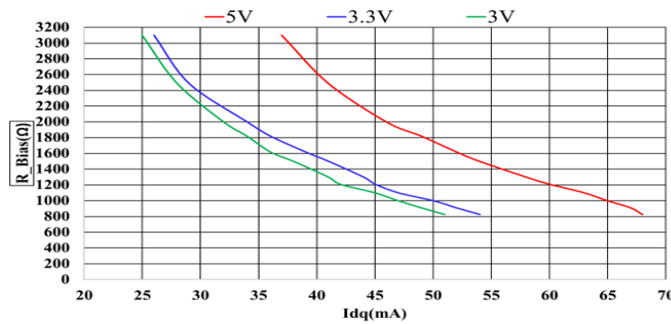
**Figure 11.3.2: Output P1dB vs Freq**



**Figure 11.3.3: Output IP3 vs Freq**



**Figure 11.3.4: Mu1 vs Freq**



**Figure 11.3.5: Rbias on Venable vs Idq**

## 12.0 Test Procedures

### Biasing Sequence

To properly bias the TL0375J-EVB-A, follow these steps:  
Connect the supply Ground the Ground test point.

- Apply bias to the Venable=5V test points.
- Apply bias to the Vdd=5V test point.
- Apply an RF input signal.

The TL0375J-EVB-A is shipped fully assembled and tested. Figure 12.1 illustrates a basic test setup diagram for evaluating s-parameters, which includes gain, input output return loss and reverse isolation using a network analyzer. Follow these steps to complete the test setup and verify the operation of the TL0375J-EVB-A:

1. Connect the Ground test point to the ground terminal of the power supply.
2. Connect the Venable and Vdd test points to the voltage output terminal of a 5 V supply that sources a current of approximately 60 mA.
3. Connect a calibrated network analyzer to the RF-in, and RF-out SMA connectors. Sweep the frequency from 1 GHz to 6 GHz and set the power to -25 dBm.

The TL0375J-EVB-A is expected to have a gain of 17.5 dB at 3.6 GHz. Refer to Figure 11.1.2 for the expected results.

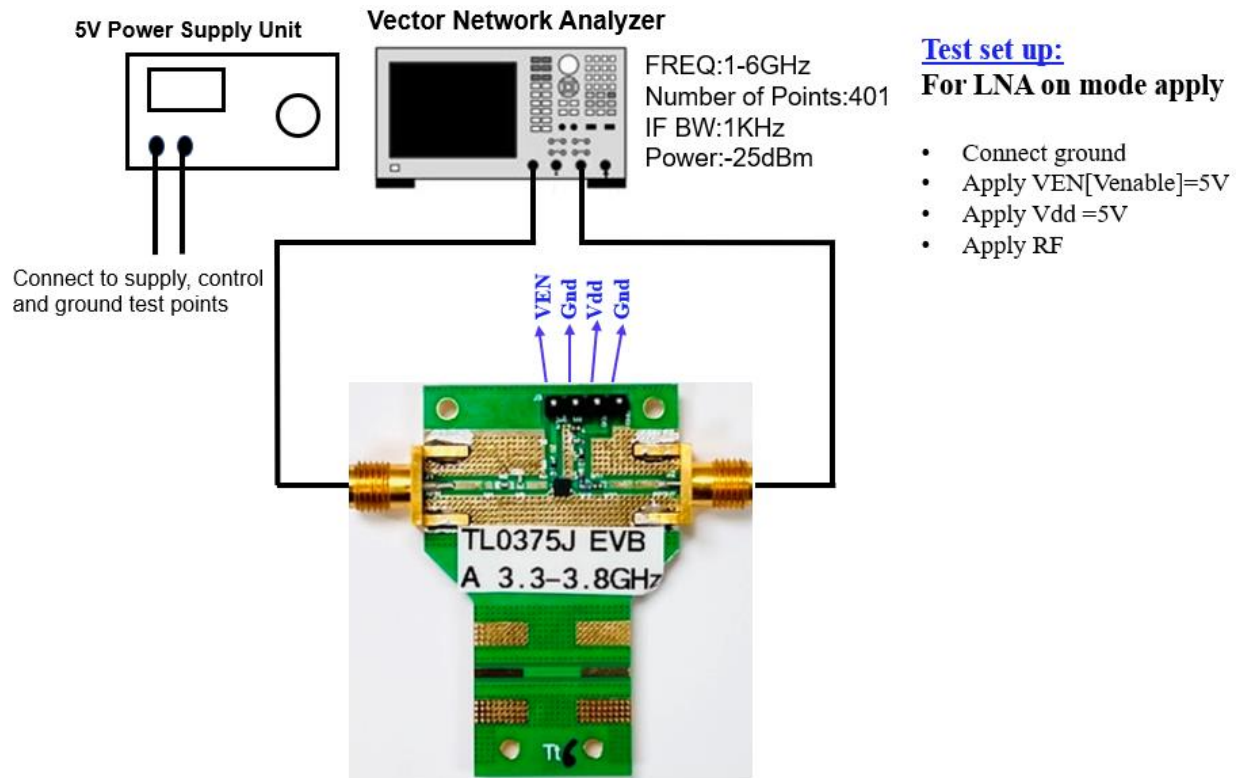
Additional test equipment is required for a comprehensive evaluation of the device's functions and performance.

For noise figure evaluation, use either a noise figure analyzer or a spectrum analyzer with a noise option. It is recommended to use a low excess noise ratio (ENR) noise source.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is recommended.

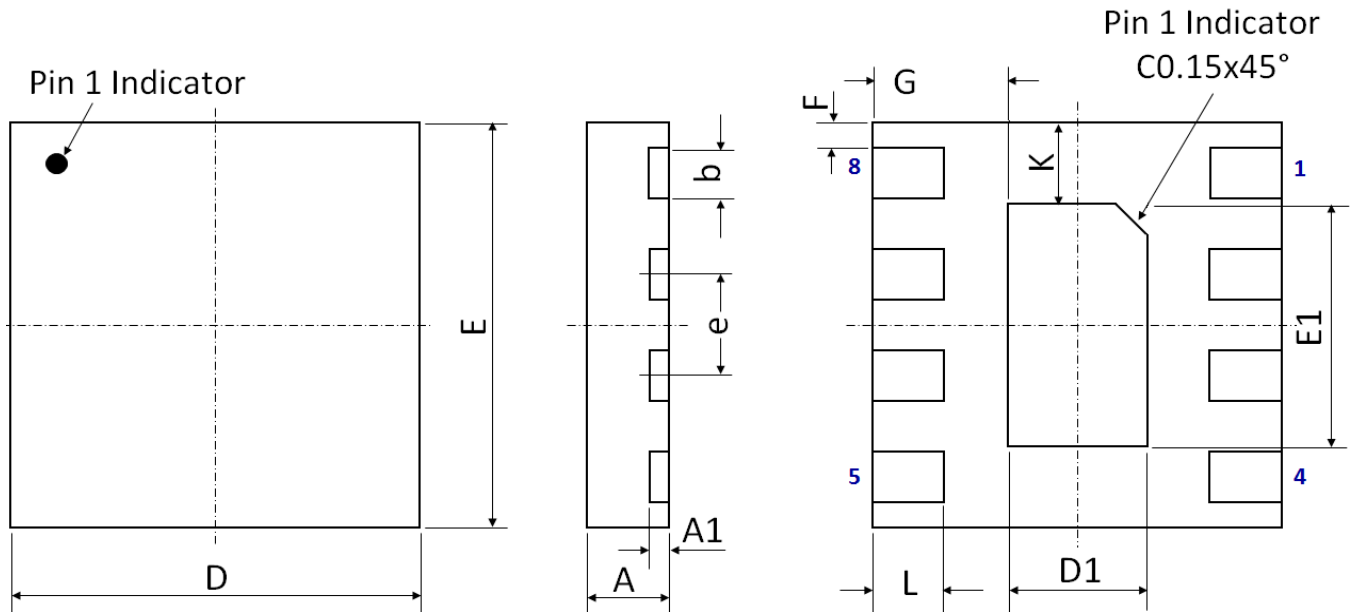
For power compression and power handling evaluations, use a two-channel power meter and a signal generator. Ensure that the input power amplifier has sufficient power capacity. Test accessories such as couplers and attenuators must also have adequate power handling capabilities.

Please note that measurements conducted at the SMA connectors of the TL0375J-EVB-A include the losses of the SMA connectors and the PCB. The through line should be measured to calibrate the effects of the TL0375J-EVB-A. The through line consists of an RF input line and an RF output line that are connected to the device and have equal lengths.



**Figure 12.1 TEST Set Up Diagram**

### 13.0 Device Package Information



**Figure 13.1 Device Package Drawing**  
(All dimensions are in mm)

**Table 13.1 Device Package Dimensions**

Dimension (mm)	Value (mm)	Tolerance (mm)	Dimension (mm)	Value (mm)	Tolerance (mm)
A	0.75	$\pm 0.05$	E	2.00 BSC	$\pm 0.05$
A1	0.203	$\pm 0.02$	E1	1.20	$\pm 0.05$
b	0.25	$\pm 0.02$	F	0.125	$\pm 0.02$
D	2.00 BSC	$\pm 0.05$	G	0.66	$\pm 0.03$
D1	0.68	$\pm 0.03$	L	0.35	$\pm 0.05$
e	0.50 BSC	$\pm 0.05$	K	0.40	$\pm 0.05$

**Note:** Lead finish: Pure Sn without underlayer; Thickness:  $7.5\mu\text{m} \sim 20\mu\text{m}$  (Typical  $10\mu\text{m} \sim 12\mu\text{m}$ )

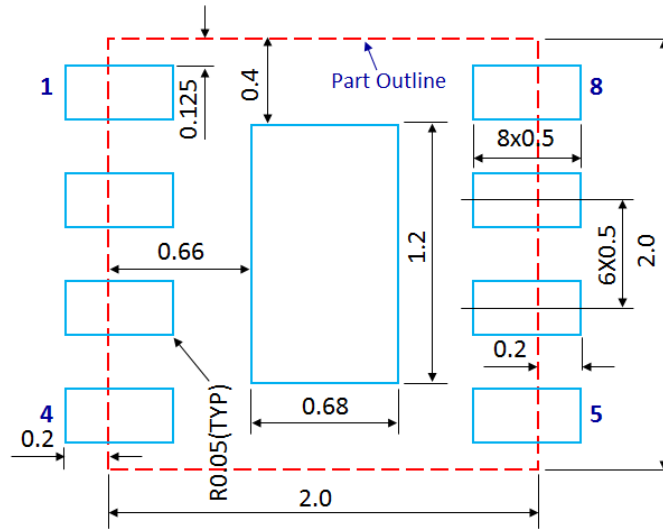
**Attention:**

Please refer to application notes *TN-001* and *TN-002* at <http://www.tagoretech.com> for PCB and soldering related guidelines.

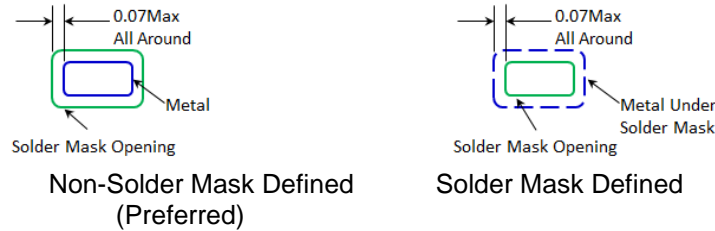
### 14.0 PCB Land Design

**Guidelines:**

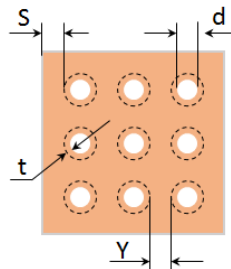
- [1] 2-layer PCB is recommended
- [2] Via diameter is recommended to be 0.3mm to prevent solder wicking inside the vias
- [3] Thermal vias shall only be placed on the center pad and should be filled/plugged with solder or copper
- [4] The maximum via number for the center pad is  $1(X) \times 2(Y) = 2$



**Figure 14.1 PCB Land Pattern**  
(Dimensions are in mm)



**Figure 14.2 Solder Mask Pattern**  
(Dimensions are in mm)



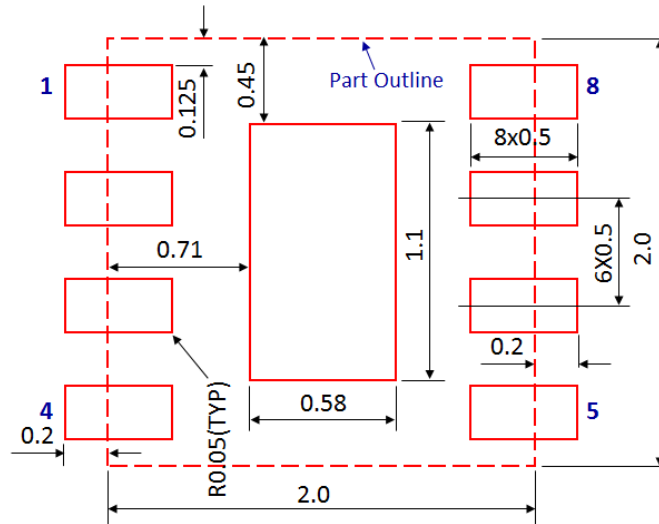
**Figure 14.3 Thermal Via Pattern**  
(Recommended Values:  $S \geq 0.15\text{mm}$ ;  $Y \geq 0.20\text{mm}$ ;  $d = 0.3\text{mm}$ ; Plating Thickness  $t = 25\mu\text{m}$  or  $50\mu\text{m}$ )

## 15.0 PCB Stencil Design

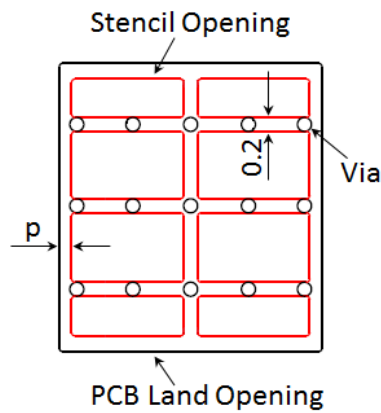
### Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125 $\mu$ m.



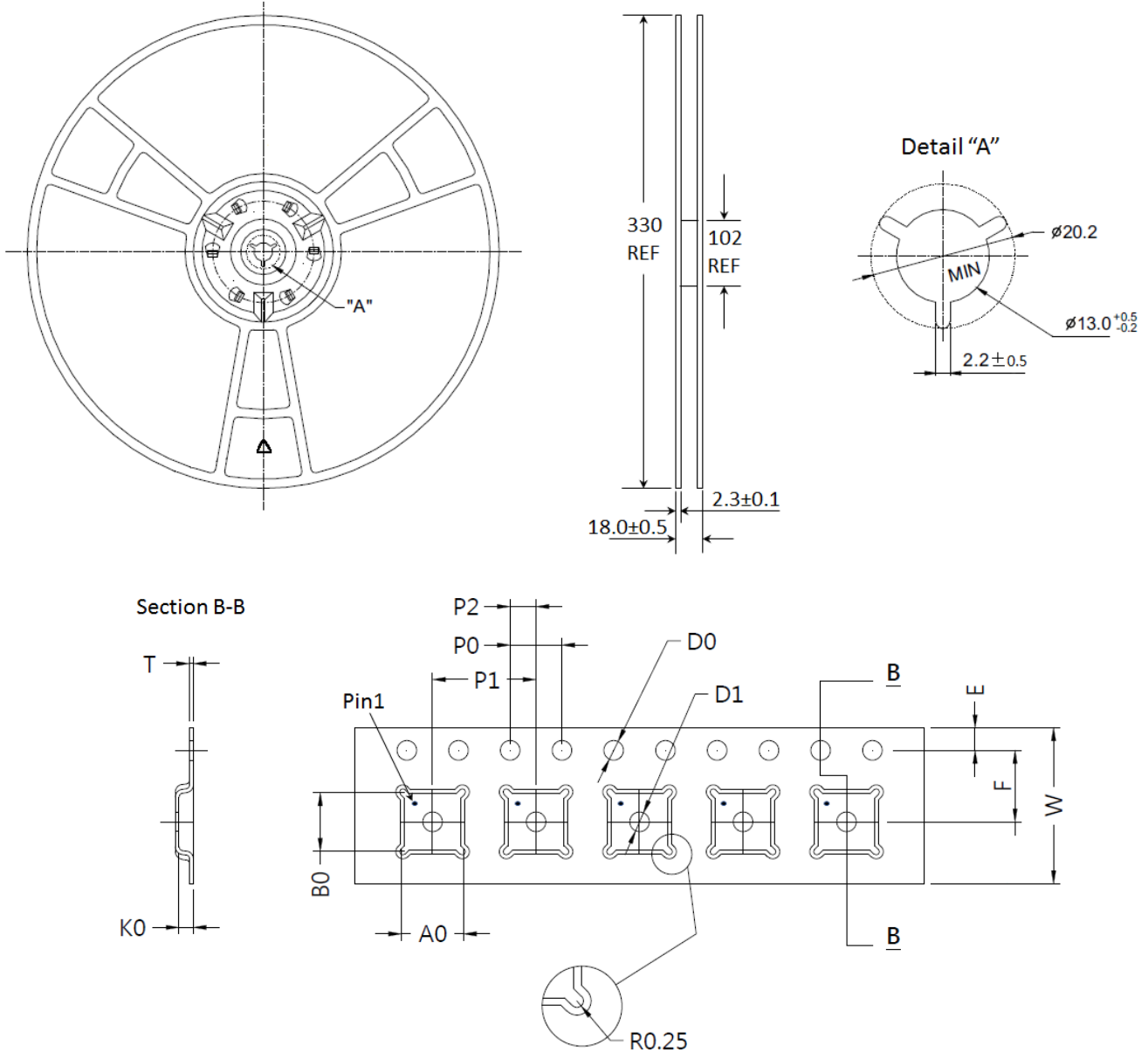
**Figure 15.1 Stencil Openings**  
(Dimensions are in mm)



**Figure 15.2 Stencil Openings Shall Not Cover Via Areas If Possible**  
(Dimensions are in mm)



**16.0 Tape and Reel Information**



**Figure 16.1 Tape and Reel Drawing**

**Table 16.1 Tape and Reel Dimensions**

Dimension (mm)	Value (mm)	Tolerance (mm)	Dimension (mm)	Value (mm)	Tolerance (mm)
A0	2.35	±0.10	K0	1.10	±0.10
B0	2.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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