TR0329M: 2.0 – 4.2 GHz Ultra Low Noise 2 Stage Bypassed LNA

1.0 Features

- Small signal gain @ 3600MHz: 34dB (High Gain mode)
  @ 3600MHz: 15dB (Low Gain mode)
- NF @ 3600MHz: 0.5dB (High Gain mode)
  @ 3600MHz: 0.5dB (Low Gain mode)
- P1dB @ 3600MHz: 20dBm (High Gain mode)
  @ 3600MHz: 10.5dBm (Low Gain mode)
- 5V Typical operating voltage
- Operating frequency: 2.0 to 4.0GHz

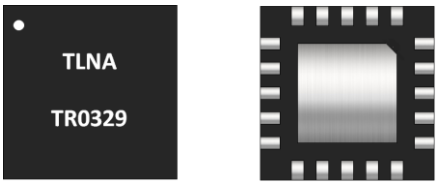

Figure 1.1 Device Image
(20 Pin 3.5×3.5×0.75mm QFN Package)

2.0 Applications

- 4G/5G Infrastructure Radios
- Small Cells and Cellular Repeaters
- Phase Array Radar
- SDARS

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TR0329M is a high-linearity, ultra-low noise 2-stage gain block amplifier module with internal 50ohm input output matching with a bypass mode functionality integrated to the second stage in the product. At 3.6 GHz, the amplifier, under high gain mode, typically provides 34dB gain, +35dBm OIP3, and 0.5 dB noise figure while drawing 90 mA current from a +5 V supply. The component also provides high performance in the low gain mode with 15dB gain, 0.5dB noise figure and +22dBm OIP3 while drawing 50 mA current.

The TR0329M is packaged in a compact, low-cost Quad Flat No Lead (QFN) 3.5x3.5x0.75mm, 20 pin plastic packages.

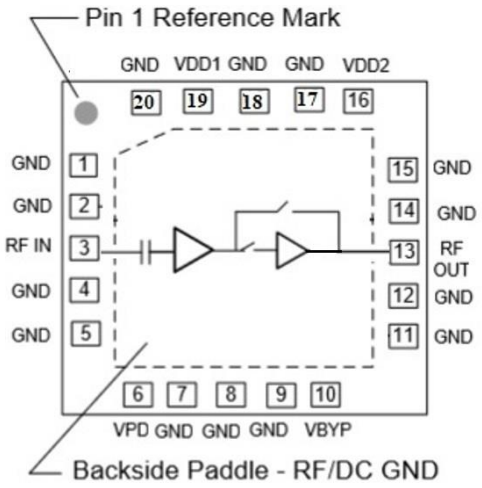

Figure 3.1 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 4.1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TR0329M	20 Pin 3.5×3.5×0.75mm QFN	Tape and Reel	5000	13" (330mm)	18mm	TR0329MTRPBF
Tuned Evaluation Board, 3300 - 4000MHz						TR0329M-EVB-A
Tuned Evaluation Board, 2300 - 2700MHz						TR0329M-EVB-B

5.0 Pin Description

Table 5.1 Pin Definition

Pin Number	Pin Name	Description
1,2,4,5,7-9,11,12,14,15,17 &18	NC/GND	No internal connection, can be connected to ground
3	RF_{IN}	RF Input. DC blocking cap required
13	RF_{OUT}	RF Output.
19	VDD1	Vdd1 supplied through an external choke inductor
16	VDD2	Vdd2 supplied through an external choke inductor
6	VPD	+5V on this pin will shut down both the LNAs.
10	VBYP	+5V on this pin keep LNA1 on & LNA2 off. In 0V both LNAs on.
Package Base	Paddle/Slug	DC and RF Ground. Also provides thermal relief. Multiple vias are recommended

Note: [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heatsinking required.

6.0 Absolute Maximum Rating

Table 6.1 Absolute Maximum Rating @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Supply voltages	VDD1 & VDD2	+6	V
RF input power CW	RF_{IN}	23	dBm
Storage Temperature Range	T_{st}	-55 to +150	°C
Operating Temperature Range	T_{op}	-40 to +105	°C
Maximum Junction Temperature	T_J	170	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	15.0	°C/W

Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:
Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Recommended DC Operating Conditions

Table 7.1 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltages	VDD1		+5.0		V
	VDD2		+5.0		
Drain Bias Currents	$I_{DQ1,}$ Set by external drain feed	40	50		mA
	$I_{DQ2,}$ Set by external drain feed	80	90		
Operating Temperature Range		-40	+25	+105	°C

8.0 RF Electrical Specifications for EVBs

Table 8.1 3300 – 4000MHz EVB A: @T_A=+25°C Unless Otherwise Specified; Venable = High

Parameter	Test Condition	Typical Values	Unit
Operational frequency Range		3.3-4.0	GHz
Gain	HG: LNAs on Bypass off	36.5-32	dB
	LG: LNA1 on Bypass on	16-14.3	dB
Noise Figure (De-embedded)	HG: LNAs on Bypass off	0.5-0.8	dB
	LG: LNA1 on Bypass on	0.5-0.8	dB
EVB Noise Figure	HG: LNAs on Bypass off	0.6-0.9	dB
	LG: LNA1 on Bypass on	0.7-0.9	dB
Input Return Loss	HG: LNAs on Bypass off	Less than -9	dB
	LG: LNA1 on Bypass on	Less than -14	dB
Output Return Loss	HG: LNAs on Bypass off	Less than -13	dB
	LG: LNA1 on Bypass on	Less than –8.3	dB
OP1dB	HG: LNAs on Bypass off	19-20.5	dBm
	LG: LNA1 on Bypass on	9-11	dBm
OIP3 (With 1MHz tone spacing)	0dBm per tone,	33-36	dBm
	-2dBm per tone,	19-22	dBm
Current, Id	HG	90	mA
	LG	45	
	PD	5	

Isolation between RFIN and RF-out PD mode ON and Bypass ON	At 3.6GHz Receive operation	50	dB
Isolation between RFIN and RF-out PD mode ON and High Gain ON		50	dB

Table 8.2 2300 – 2700MHz EVB B: @T_A=+25°C Unless Otherwise Specified; Venable = High

Parameter	Test Condition	Typical Values	Unit
Operational frequency Range		2.3-2.7	GHz
Gain	HG: LNAs on Bypass off	37-36.8	dB
	LG: LNA1 on Bypass on	18-16.7	dB
Noise Figure (De-embedded)	HG: LNAs on Bypass off	0.5-0.6	dB
	LG: LNA1 on Bypass on	0.5-0.6	dB
EVB Noise Figure	HG: LNAs on Bypass off	0.6-0.7	dB
	LG: LNA1 on Bypass on	0.6-0.7	dB
Input Return Loss	HG: LNAs on Bypass off	Less than -11	dB
	LG: LNA1 on Bypass on	Less than -11	dB
Output Return Loss	HG: LNAs on Bypass off	Less than -11	dB
	LG: LNA1 on Bypass on	Less than –5.5	dB
OP1dB	HG: LNAs on Bypass off	17-18.5	dBm
	LG: LNA1 on Bypass on	10-12	dBm
OIP3 (With 1MHz tone spacing)	0dBm per tone,	30-31	dBm
	-2dBm per tone,	21-23	dBm
Current, Id	HG	90	mA
	LG	45	
	PD	5	
Isolation between RFIN and RF-out PD mode ON and Bypass ON	At 2.5GHz Receive operation	55	dB
Isolation between RFIN and RF-out PD mode ON and High Gain ON		50	dB

Table 8.2 Control Truth Table @T_A=+25°C Unless Otherwise Specified.

PD	BP	State
1	0	LNA1 OFF, LNA2 OFF, Bypass OFF
0	0	LNA1 ON, LNA2 ON Bypass ON
0	1	LNA1 ON, LNA2 OFF, Bypass ON
1	1	LNA1 OFF, LNA2 OFF, Bypass OFF

Table 8.3 Switching Speed @T_A=+25°C Unless Otherwise Specified.

PD	BP	State	50% Vctrl to 90% of RF	50% Vctrl to 10% of RF	Units
0V	0V	LNA1 ON, LNA2 ON, Bypass OFF	350	---	ns
	5V	LNA1 ON, LNA2 OFF Bypass ON	---	300	
5V	0V	LNA1 OFF, LNA2 OFF, Bypass OFF	700	430	
	5V	LNA1 OFF, LNA2 OFF, Bypass ON	320	560	

9.0 Typical Characteristics

9.1 3300 - 4000MHz tuned EVB (Low Gain mode), -40ºC,25ºC,85ºC,105 ºC, broadband

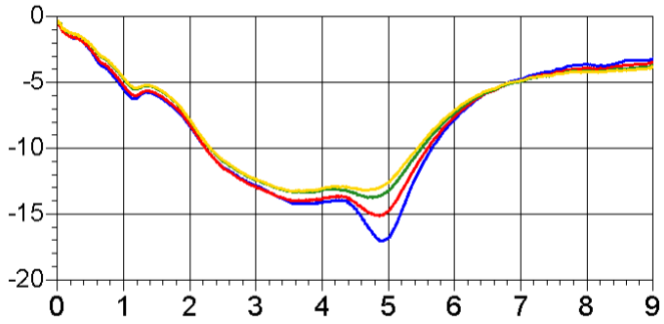

Figure 9.1.1 S11 (IRL in dB) vs Freq(GHz)

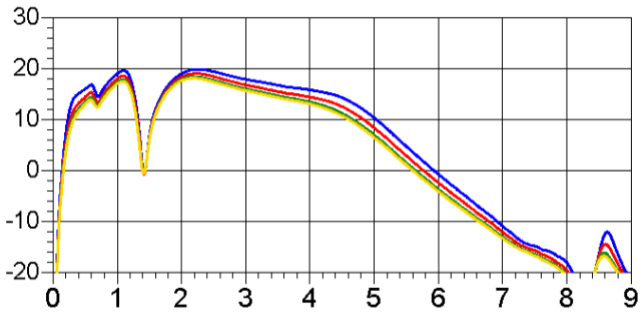

Figure 9.1.2 S21 (Gain in dB) vs Freq(GHz)

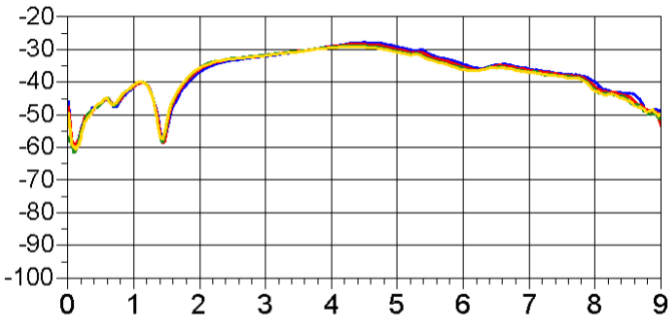

Figure 9.1.3 S12 (Rev Iso in dB) vs Freq(GHz)

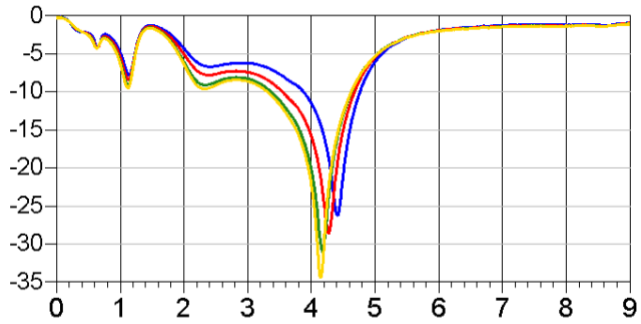

Figure 9.1.4 S22 (ORL in dB) vs Freq(GHz)

9.2 3300 - 4000MHz tuned EVB (Low Gain mode), -40ºC,25ºC,85ºC,105 ºC, narrowband

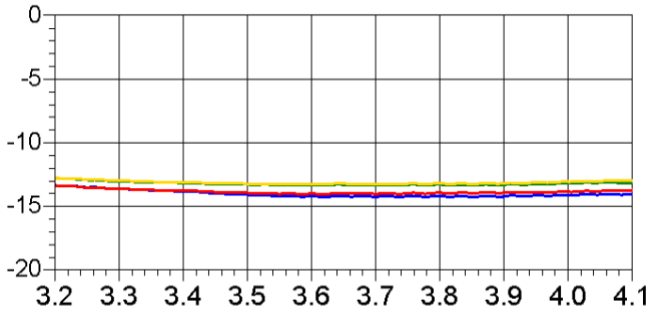

Figure 9.2.1 S11 (IRL in dB) vs Freq(GHz)

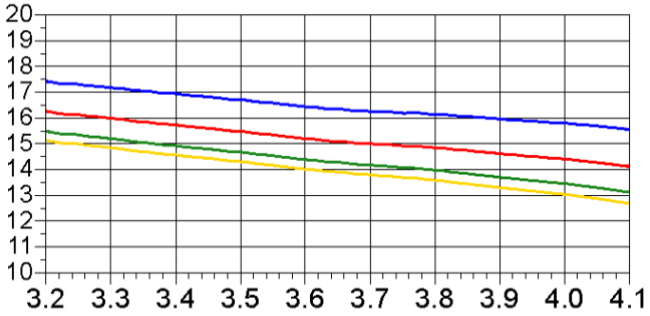

Figure 9.2.2 S21 (Gain in dB) vs Freq(GHz)

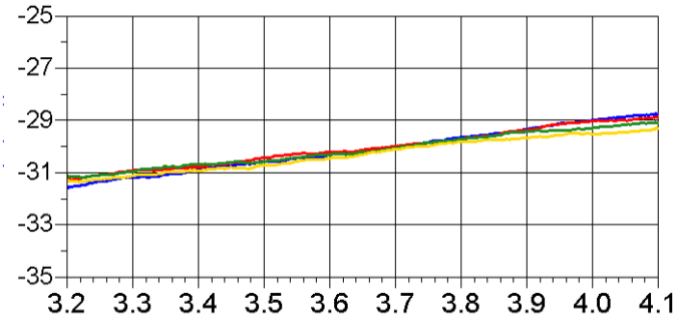

Figure 9.2.3 S12 (Rev Iso in dB) vs Freq(GHz)

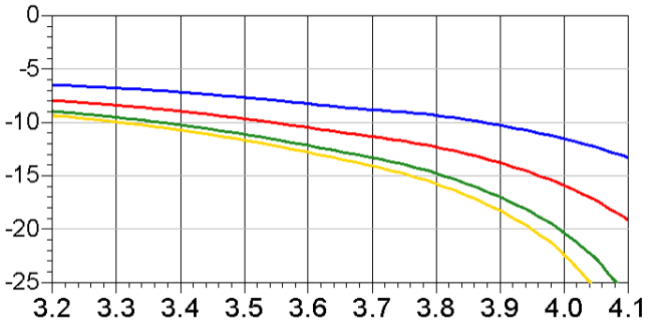

Figure 9.2.4 S22 (ORL in dB) vs Freq(GHz)

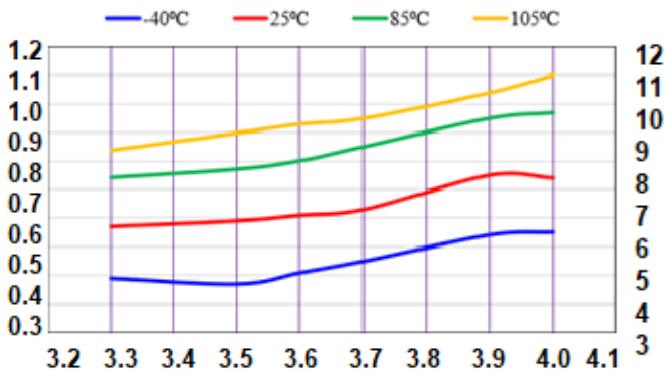

Figure 9.2.5 EVB Noise Figure (in dB) vs Freq(GHz)

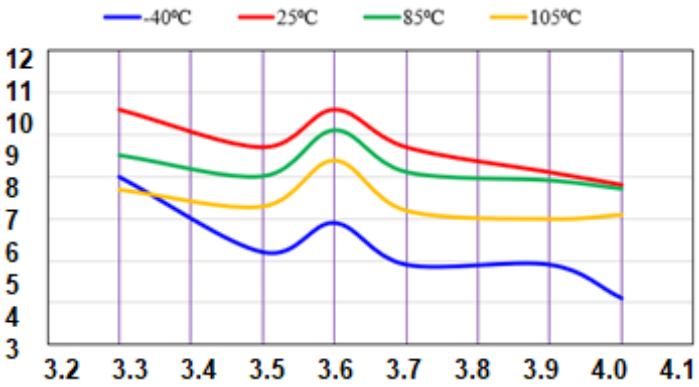

Figure 9.2.6 Output P1dB vs Freq(GHz)

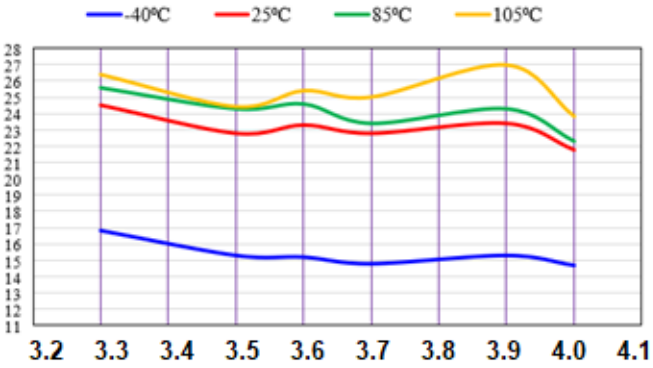

Figure 9.2.7 Output IP3 (in dBm) vs Freq(GHz)

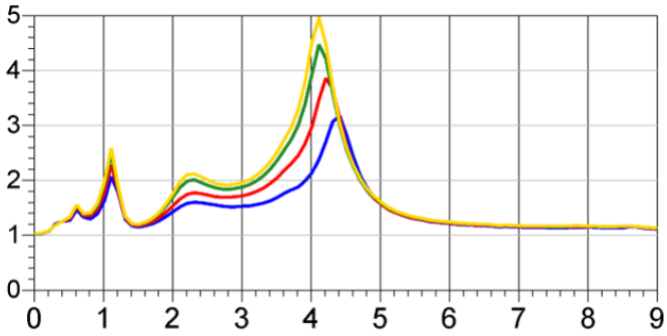

Figure 9.2.8 Mu1 vs Freq(GHz)

9.3 3300 - 4000MHz tuned EVB (High Gain mode), -40ºC,25ºC,85ºC,105 ºC, broadband

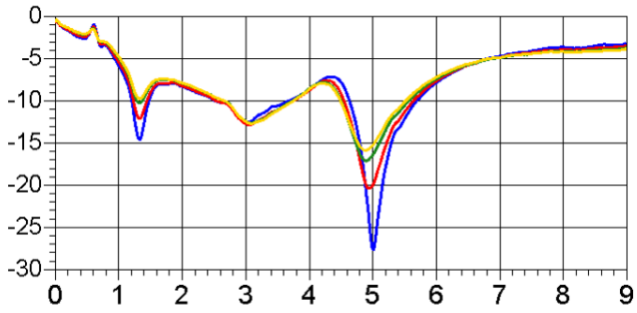

Figure 9.3.1 S11 (IRL in dB) vs Freq(GHz)

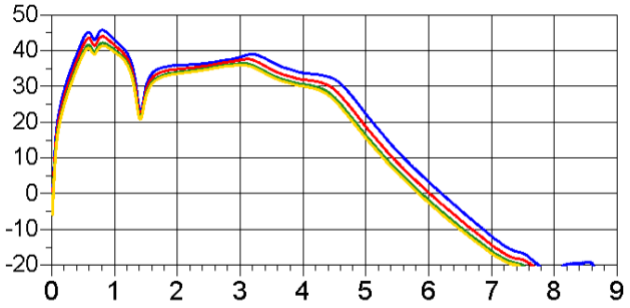

Figure 9.3.2 S21 (Gain in dB) vs Freq(GHz)

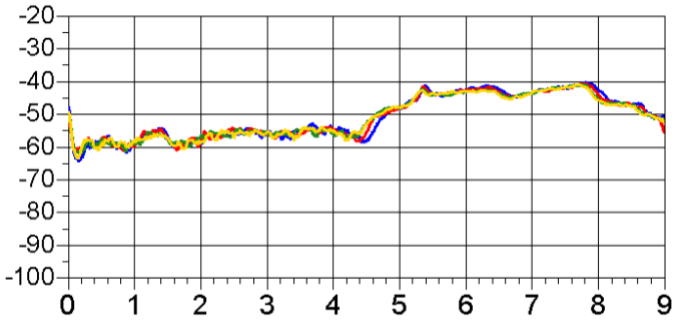

Figure 9.3.3 S12 (Rev Iso in dB) vs Freq(GHz)

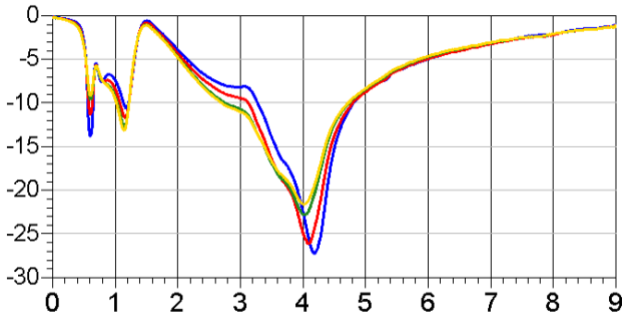

Figure 9.3.4 S22 (ORL in dB) vs Freq(GHz)

9.4 3300 - 4000MHz tuned EVB (High Gain mode), -40ºC,25ºC,85ºC,105 ºC, narrowband

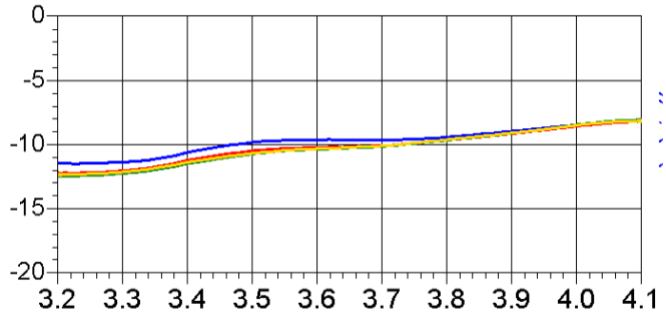

Figure 9.4.1 S11 (IRL in dB) vs Freq Freq(GHz)

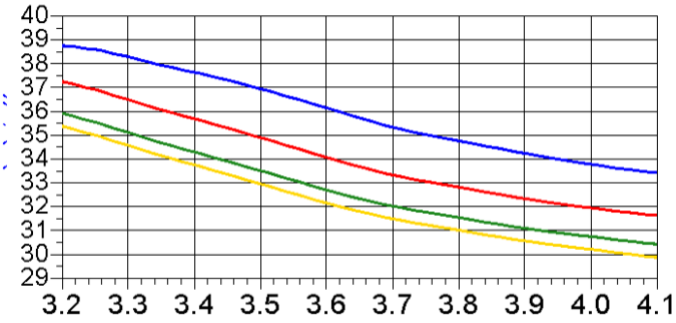

Figure 9.4.2 S21 (Gain in dB) vs Freq Freq(GHz)

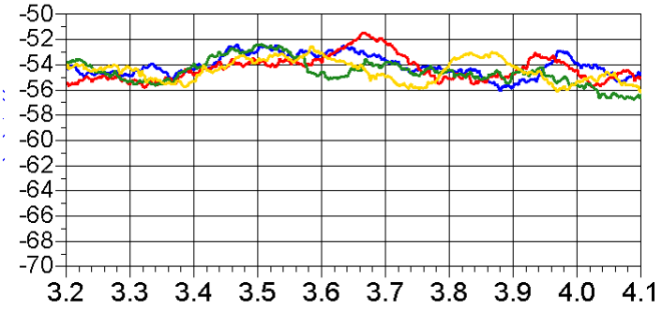

Figure 9.4.3 S12 (Rev Iso in dB) vs Freq(GHz)

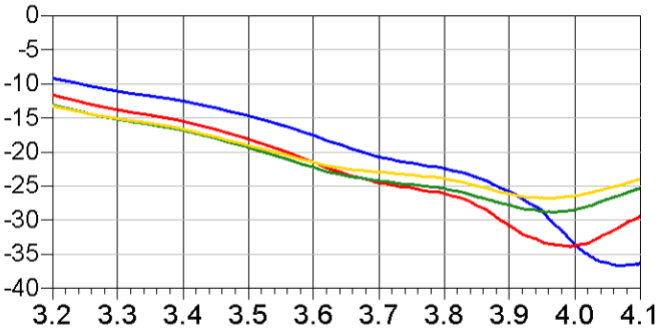

Figure 9.4.4 S22 (ORL in dB) vs Freq(GHz)

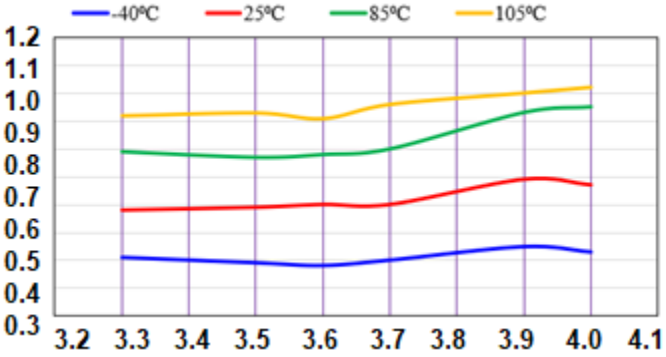

Figure 9.4.5 EVB Noise Figure (in dB) vs Freq(GHz)

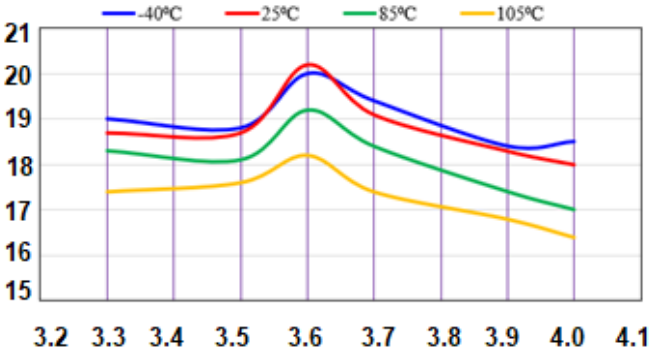

Figure 9.4.6 Output P1dB vs Freq(GHz)

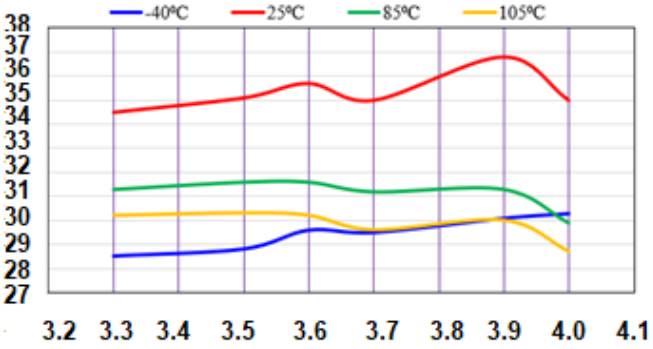

Figure 9.4.7 Output IP3(in dBm) vs Freq(GHz)

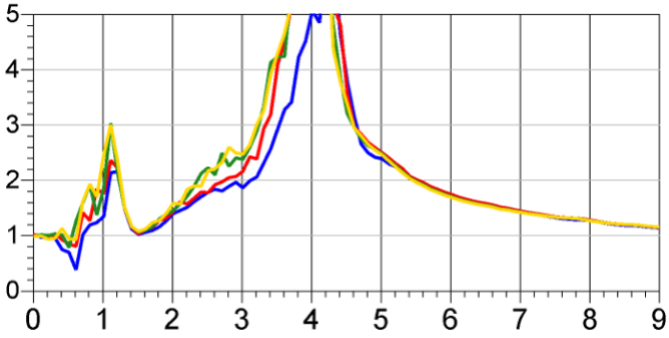

Figure 9.4.8 Mu1 vs Freq(GHz)

10.0 Evaluation Boards

10.1 3300 - 4000MHz EVB A

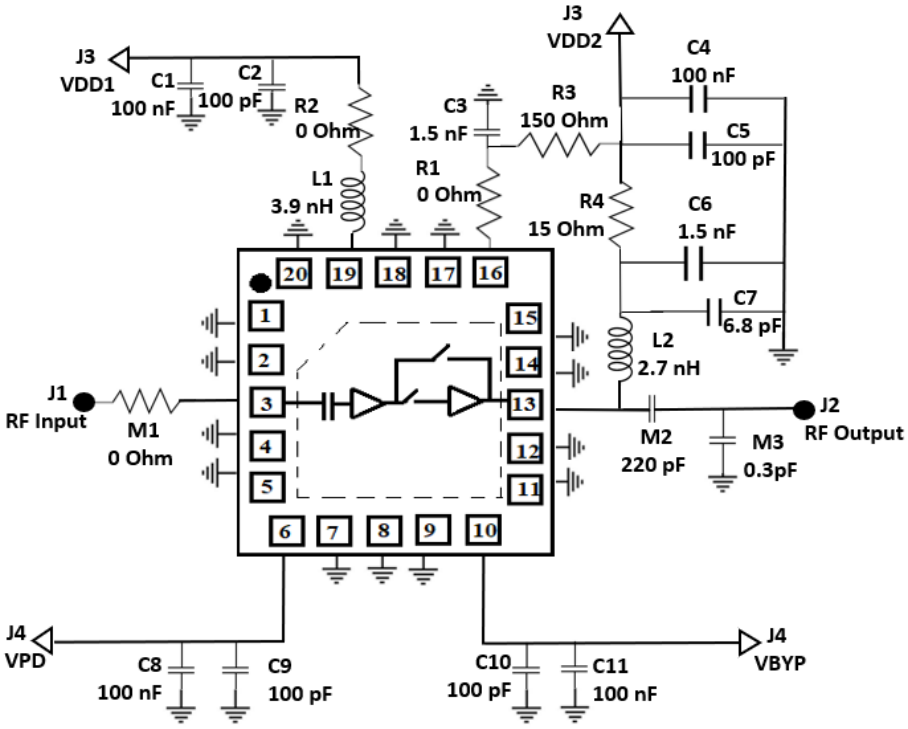

Figure 10.1 Schematic of the 3300-4000MHz EVB-A

Table 10.1 BOM of the 3300-4000MHz EVB A

Component ID	Value	Manufacturer	Recommended Part Number	Qty
M1, R1, R2	0Ω	Panasonic	ERJ-2GE0R00X	3
C7	6.8pF	Murata	GJM1555C1H6R8BB01D	1
M2	220pF	Kemet	C0402C221K5GACAUTO	1
C2, C5, C9, C10	100pF	AVX	04025A101JAT4A	4
C1, C4, C8, C11	100nF	TDK	C1005X7R1H104K050BE	4
L1	3.9 nH	Coil craft / Wurth Electronics	0402HP-3N9XGE / 744916039	1
C3, C6	1.5nF	Murata	04025C152JAT2A	2
L2	2.7 nH	Coil craft / Wurth Electronics	0402HP-2N7XGE / 744916027	1
R4	15 Ω	Panasonic	ERJ-H2RD15R0X	1
R3	150Ω	Panasonic	ERJ-2RHD1500X	1
M3	0.3pF	Murata	GJM1555C1HR30BB01	1
PCB	Rogers RO4350B, 20 mils, 1 oz copper			1

10.1 2300 - 2700MHz EVB B

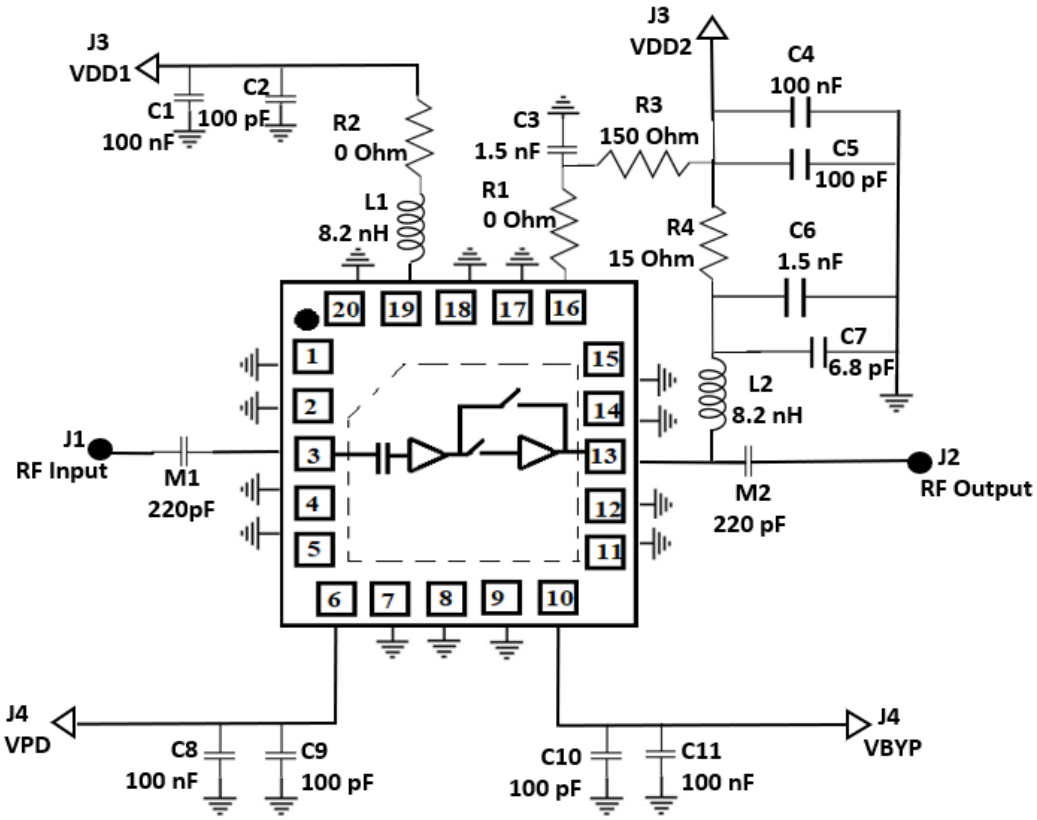

Figure 10.1 Schematic of the 2300-2700MHz EVB-B

Table 10.1 BOM of the 2300-2700MHz EVB B

Component ID	Value	Manufacturer	Recommended Part Number	Qty
R1, R2	0Ω	Panasonic	ERJ-2GE0R00X	2
C7	6.8pF	Murata	GJM1555C1H6R8BB01D	1
M2	220pF	Kemet	C0402C221K5GACAUTO	1
C2, C5, C9, C10	100pF	AVX	04025A101JAT4A	4
C1, C4, C8, C11	100nF	TDK	C1005X7R1H104K050BE	4
L1, L2	8.2 nH	Coil craft / Wurth Electronics	0402HP-8N2XGE / 744916039	2
R4	15 Ω	Panasonic	ERJ-H2RD15R0X	1
R3	150Ω	Panasonic	ERJ-2RHD1500X	1
C3, C6	1.5nF	Murata	04025C152JAT2A	2
PCB	Rogers RO4350B, 20 mils, 1 oz copper			1

11.0 Device Package Information

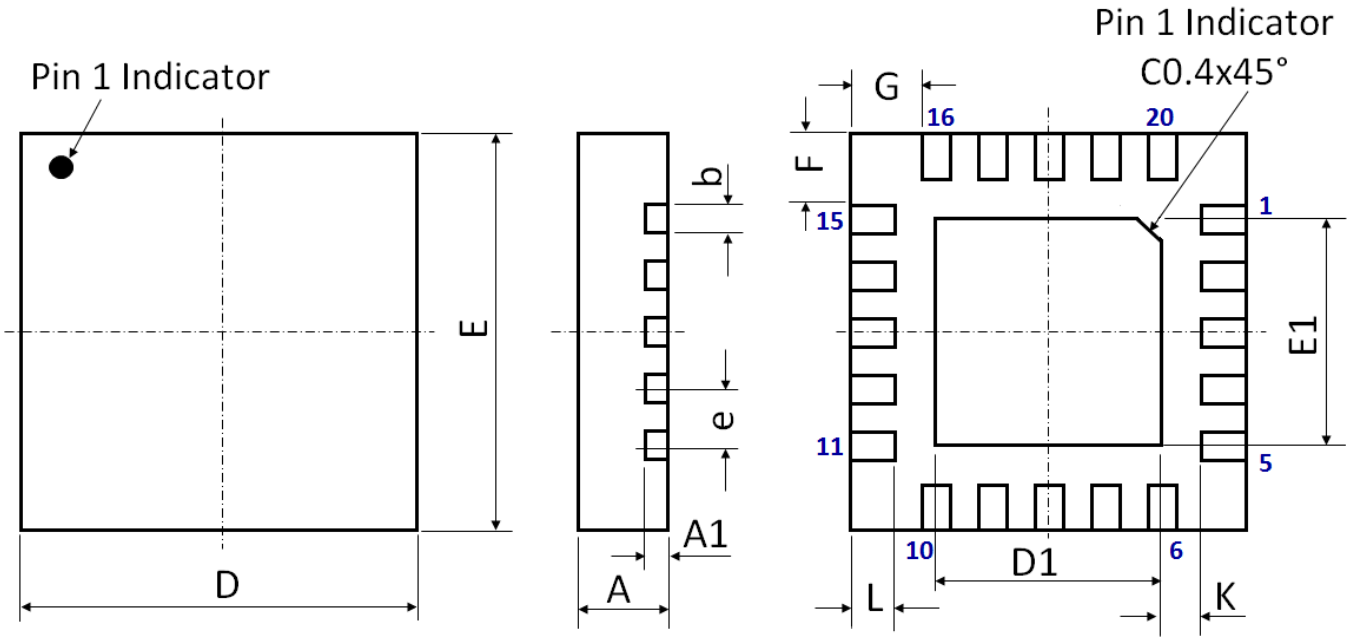

Figure 11.1 Device Package Drawing
(All dimensions are in mm)

Table 11.1 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.75	±0.05	E	3.50 BSC	±0.05
A1	0.203	±0.02	E1	2.00	±0.05
b	0.25	±0.02	F	0.625	±0.02
D	3.50 BSC	±0.05	G	0.625	±0.03
D1	2.00	±0.03	L	0.40	±0.05
e	0.50 BSC	±0.05	K	0.35	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

12.0 PCB Land Design

Guidelines:
[1] 2-layer PCB is recommended
[2] Via diameter is recommended to be 0.3mm to prevent solder wicking inside the vias
[3] Thermal vias shall be placed on the center pad
[4] The maximum via number for the center pad is **3(X)×3(Y)=9**

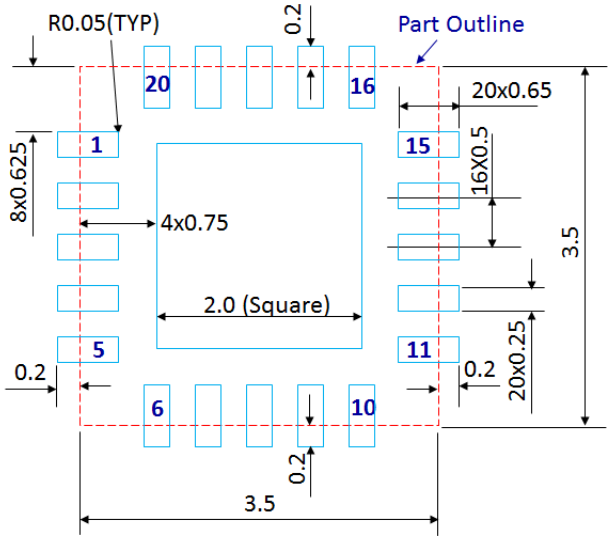

Figure 12.1 PCB Land Pattern
(Dimensions are in mm)

Non-Solder Mask Defined
(Preferred)

Solder Mask Defined

Figure 12.2 Solder Mask Pattern
(Dimensions are in mm)

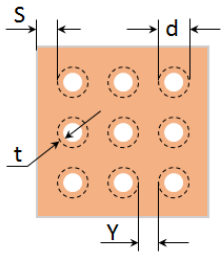

Figure 12.3 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.3mm; Plating Thickness t=25μm or 50μm)

13.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125μm.

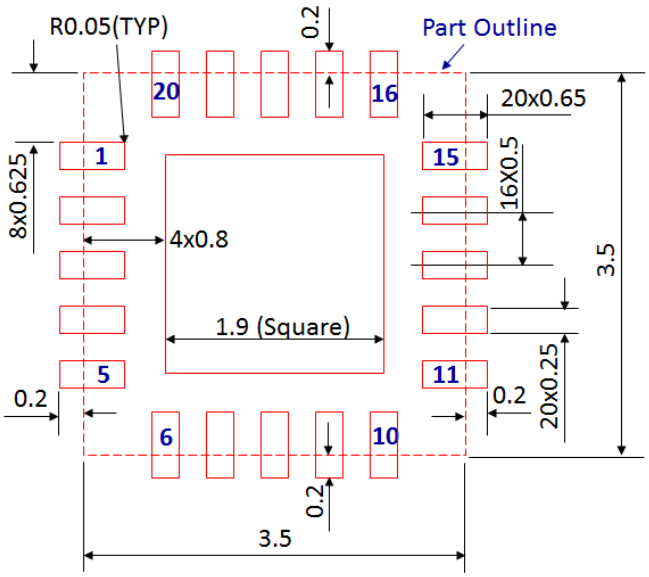

Figure 13.1 Stencil Openings
(Dimensions are in mm)

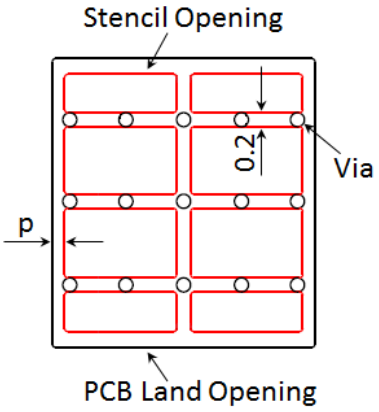

Figure 13.2 Stencil Openings Shall Not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

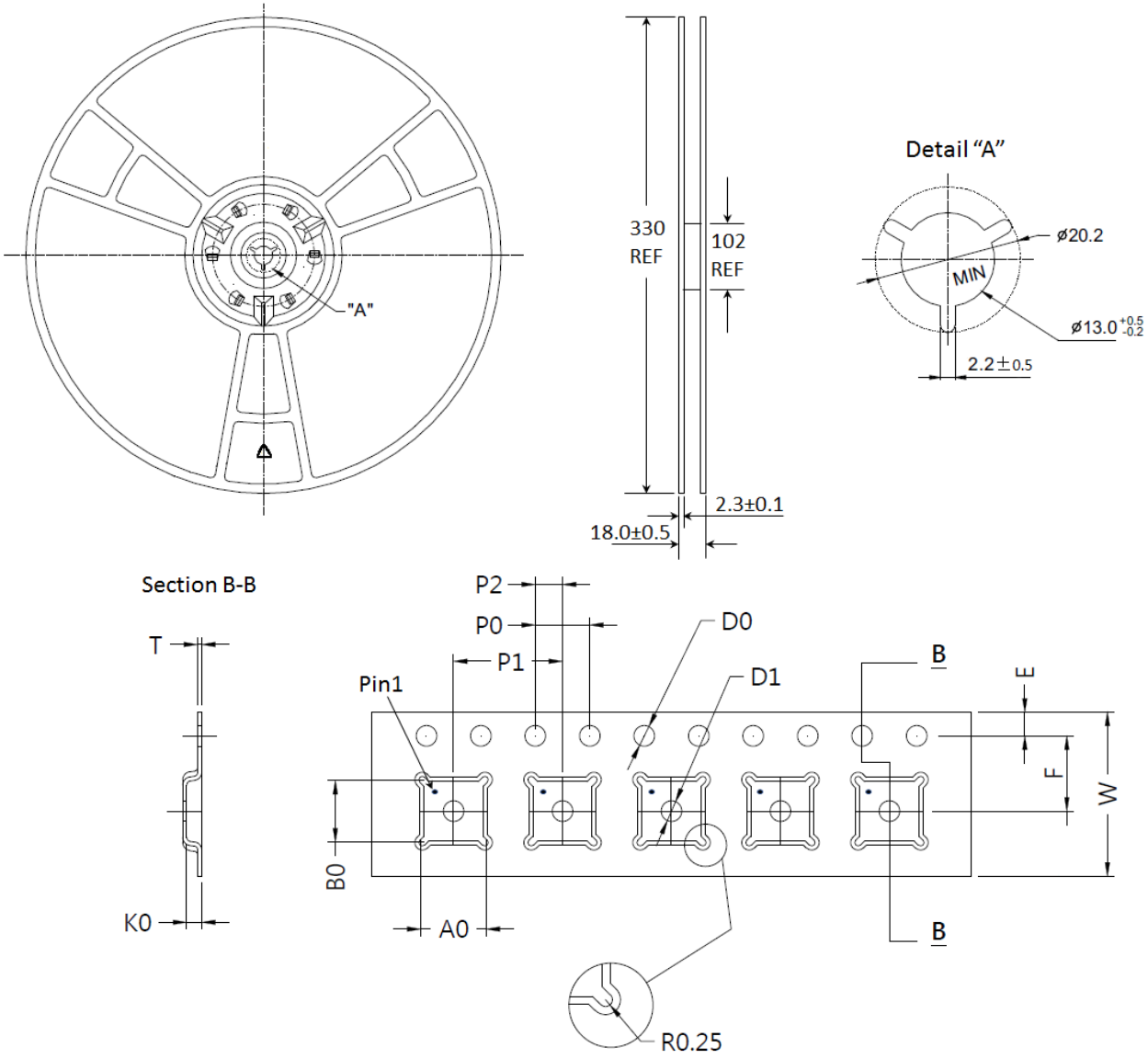

Figure 14.1 Tape and Reel Drawing

Table 14.1 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	2.35	±0.10	K0	1.10	±0.10
B0	2.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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