TS63410K – GaN Broadband RF Tuning Switch 4-Bit SP4T

1.0 Features

- Rds-on 1.1Ω
- Coff 0.21pF
- RF peak voltage handling of 100V
- 4-BIT 16 possible independent state configurations
- No external DC blocking capacitors on RF lines
- DC Supply: Vdd=2.6~5.5V
- 1.2~5.0V GPIO bus

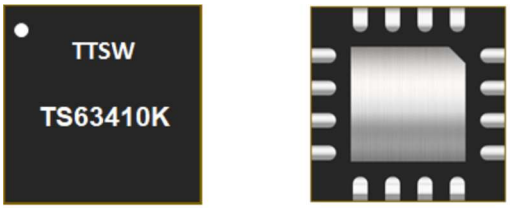


Figure 1 Device Image
(16 Pin 3×3×0.8mm QFN Package)

2.0 Applications

- Tunable RF filter, Dynamic matching, and antenna tuning
- Private mobile radio handsets
- Public safety handsets
- Cellular infrastructure and Satellite terminals
- Biomedical instruments and Implant device charging

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS63410K is a reflective open Single Pole Four Throw (SP4T) switch designed for antenna or filter tuning applications where high RF peak voltage handling is desired. TS63410K is suitable for frequency range from 1MHz to 3GHz. The TS63410K has a very low 1.1Ω on resistance and off capacitance of 0.21pF. This switch can select up to 16 independent states.

The TS63410K is packaged in a compact Quad Flat No lead (QFN) 3x3mm 16 leads plastic package.

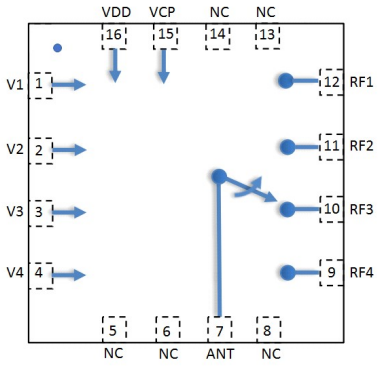


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TS63410K	16 Pin 3×3×0.8mm QFN	Tape and Reel	3000	13” (330mm)	18mm	TS63410KMTRPBF
Evaluation Board						TS63410K-EVB

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	V1	Switch control input 1
2	V2	Switch control input 2
3	V3	Switch control input 3
4	V4	Switch control input 4
5,6,8,13,14	NC	No internal connection, can be grounded
7	ANT	Antenna port
9	RF4	RF port 4
10	RF3	RF port 3
11	RF2	RF port 2
12	RF1	RF port 1
15	VCP	Add 1nF Capacitor to Gnd on this pin
16	VDD	DC power supply. Add 10nF bypass cap go Gnd close this pin

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Vdd Power Supply Max Voltage	VDD	6	V
Storage Temperature Range	T_{st}	-55 to +125	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+140	°C
RF Input Power CW, 800MHz	RFx	41	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	20	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$	≤ 39	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:
Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C; VDD=+2.7V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating Frequency		1		3000	MHz
ON Resistance	On state, DC measurement		1.1		Ω
OFF Capacitance	Total capacitance of each OFF path		0.21		pF
RF Peak Voltage	Measured at 10MHz		100		V
Insertion Loss, RFx	100MHz		0.25		dB
	500MHz		0.40		
	1.0GHz		0.45		
	2.0GHz		0.85		
	3.0GHz		1.4		
Isolation ANT-RFx	100MHz		40		dB
	500MHz		26		
	1.0GHz		20		
	2.0GHz		15		
	3.0GHz		12		
Return Loss ANT-RFx	100MHz		43		dB
	500MHz		31		
	1.0GHz		22		
	2.0GHz		15		
	3.0GHz		11		
H2	800MHz, Pin=35dBm		80		dBc
H3	800MHz, Pin=35dBm		85		dBc
IIP3	800MHz		71		dBm
P0.1dB[1]	1~10MHz		40		dBm
	10~1000MHz		42		dBm
Switching Time	50% ctrl to 10/90% of the RF value is settled. C1=1nF to Gnd on VCP		2.0		μs
Start-up Time	50% ctrl to 10/90% of the RF value is settled. C1=1nF to Gnd on VCP		TBD		μs
Control Voltage	Power supply, VDD	2.6	2.7	5.5	V
	All control pins high, V_{ih}	1.0	2.7	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control Current	All control pins low, I_{il}		0		μA
	All control pins high, I_{ih}			7.5	μA
Current Consumption, IDD	Active mode		170	200	μA

Note:

[1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

[3] Start-up time is the time from VDD ON to RF signal settled on a throw or transition time from low power mode to active mode.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	V2	V3	V4	Active RF Path
0	0	0	0	All OFF state
0	0	0	1	RF4
0	0	1	0	RF3
0	0	1	1	RF3, RF4
0	1	0	0	RF2
0	1	0	1	RF2, RF4
0	1	1	0	RF2, RF3
0	1	1	1	RF2, RF3, RF4
1	0	0	0	RF1
1	0	0	1	RF1, RF4
1	0	1	0	RF1, RF3
1	0	1	1	RF1, RF3, RF4
1	1	0	0	RF1, RF2
1	1	0	1	RF1, RF2, RF4
1	1	1	0	RF1, RF2, RF3
1	1	1	1	All ON state

Attention:

[1] VDD should be applied first before V1, V2, V3 and V4, otherwise may cause damage to the device.

[2] There are internal pull-downs to ground on all control pins, the state at start-up without any control voltage applied will be All OFF.

[3] If there is no DC path to ground on the ANT-to-RF port paths, the switch will not change its state. Consult Section 12.0 for more details.

9.0 Evaluation Board

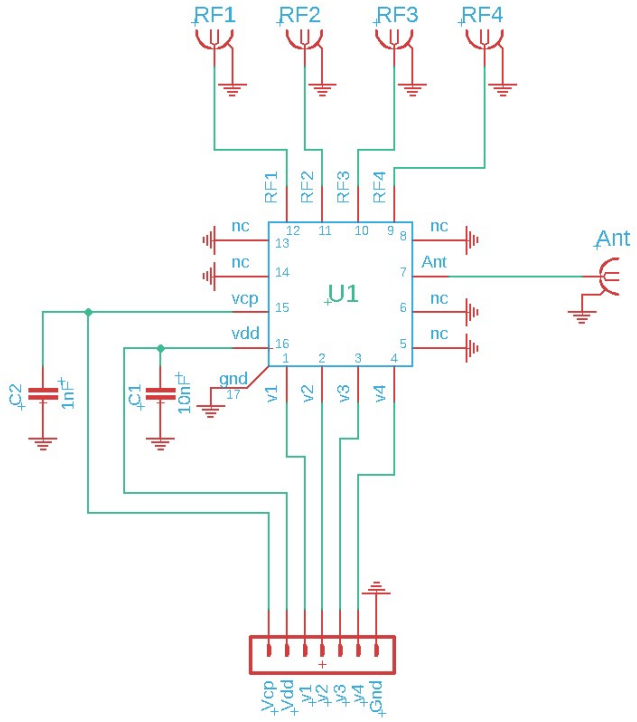


Figure 3: Evaluation Board Schematic

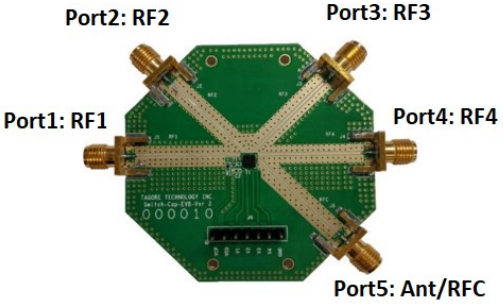


Figure 4: Evaluation Board Image

10.0 Typical Characteristics

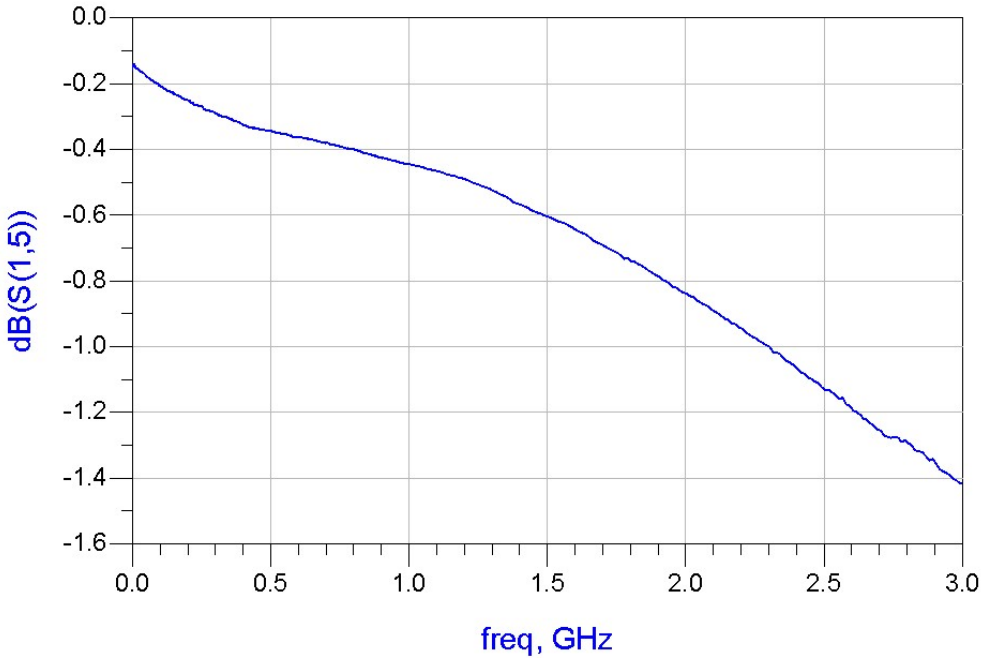


Figure 5: Insertion Loss between RF1-Ant for RF1-On State 0001

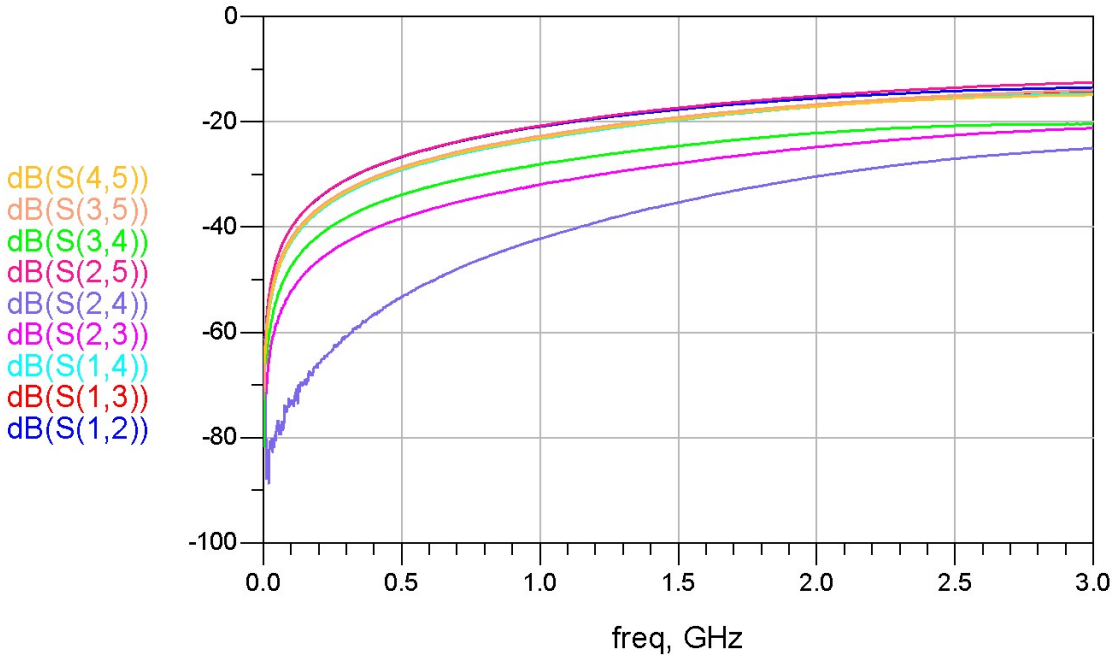


Figure 6: All Port-Port Isolations for RF1-On State 0001

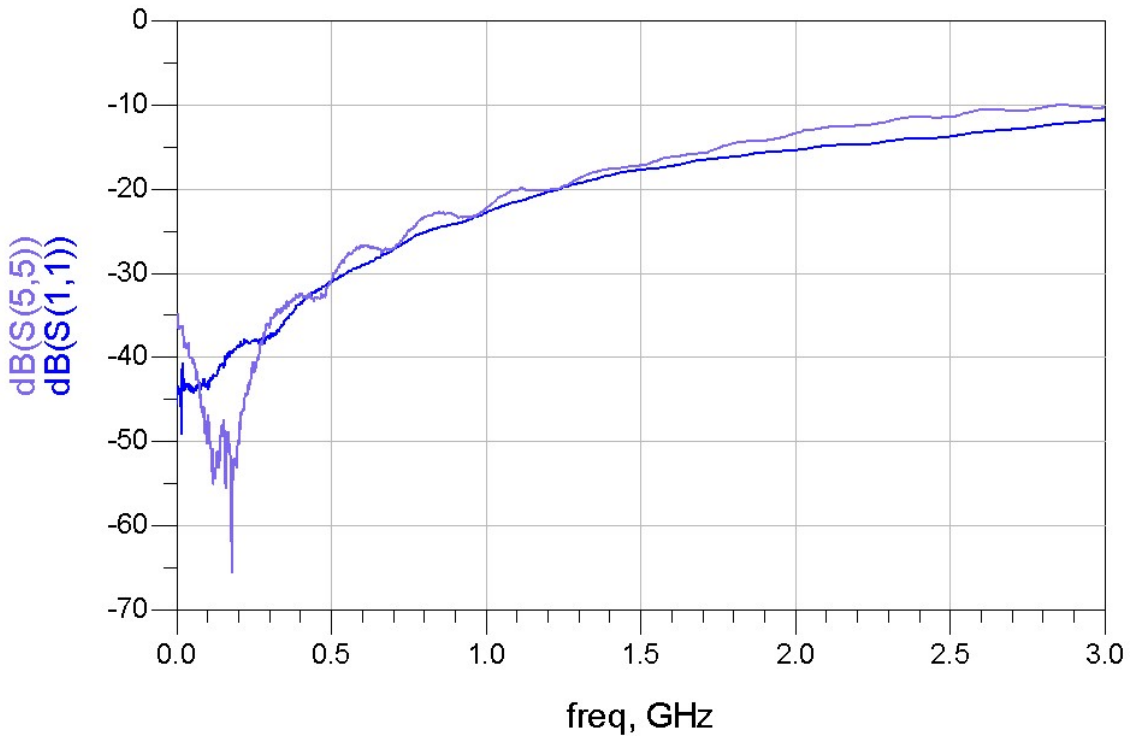


Figure 7: On Port Return Loss for RF1 and Ant port for RF1-On State 0001

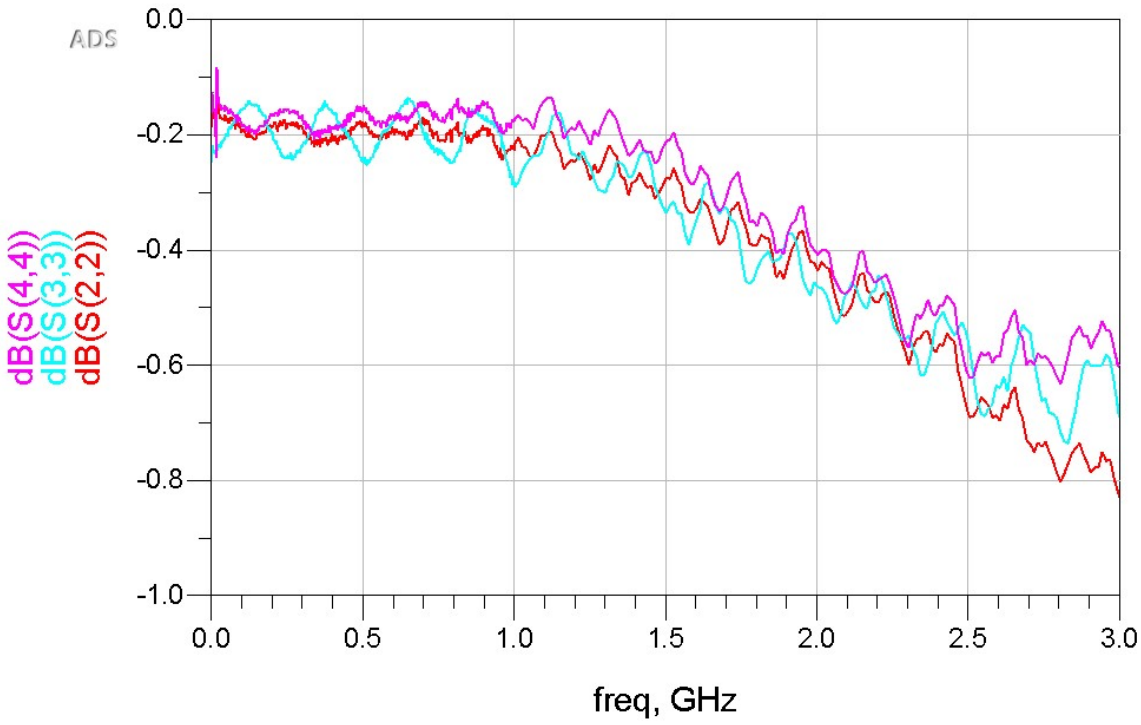


Figure 8: Off Port Return Loss for RF1-On State 0001

11.0 Internal Circuit Diagram

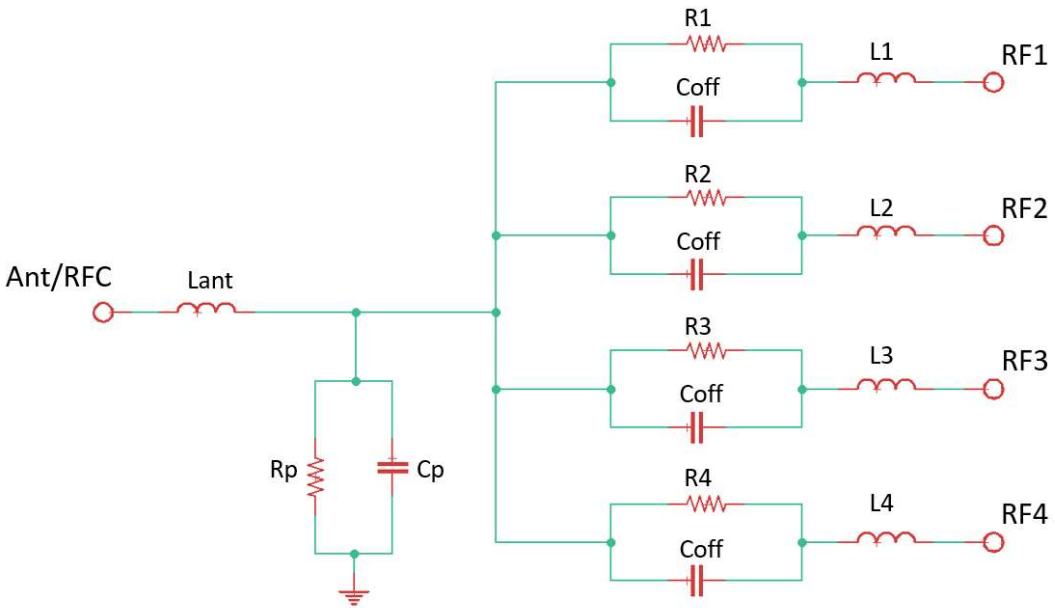


Figure 9: Simplified Circuit Diagram

Component	Value	Unit
Rp	12.5K	Ω
Cp	0.95	pF
Coff	0.21	pF
R1-R4	1.1 if ON State	Ω
	78K if OFF State	Ω
Lant	0.9	nH
L1-L4	0.6	nH

Note: Ron/Off is measured at DC. The circuit model is general purpose model, and will not accurately predict full performance, such as Q and losses in a tunable filter or antenna design. For more accuracy, it is recommended to use a customized s-parameter model which is available for download:

SP4T tuning switch simulation model

Available for download

- Derived 5 Port touchstone S-parameter model file
- 16 total .S5P files for all 4-bit state combinations
- Notes:
  - Frequency up to 3GHz
  - Accurately predict Q and losses
  - Compatible with ADS/Microwave Office
  - EM simulation of PCB is recommended
  - Accurate models of external components such as inductors and capacitors is required

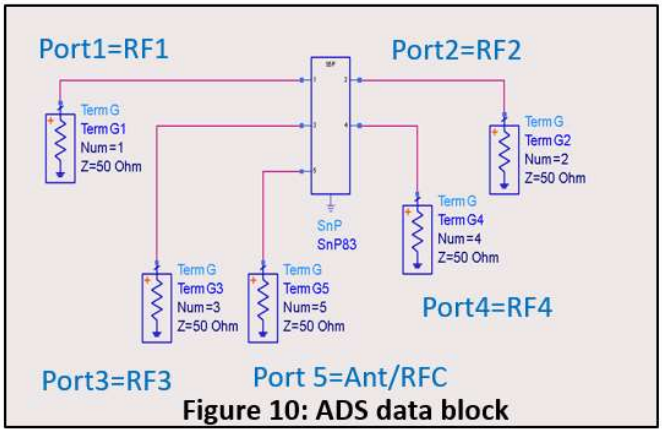


Figure 10: ADS data block

Application Board 1: Tunable Band-Pass Filter 280-500MHz (1 Switch, 1 pole LC resonator)

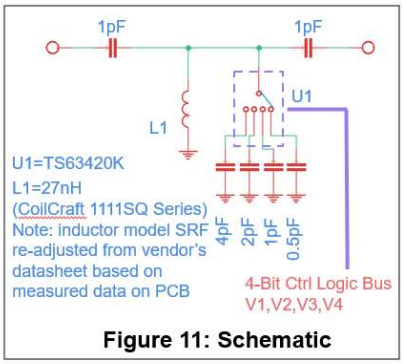


Figure 11: Schematic

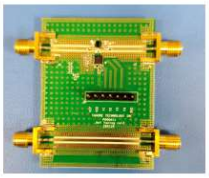


Figure 12: Evaluation Board1

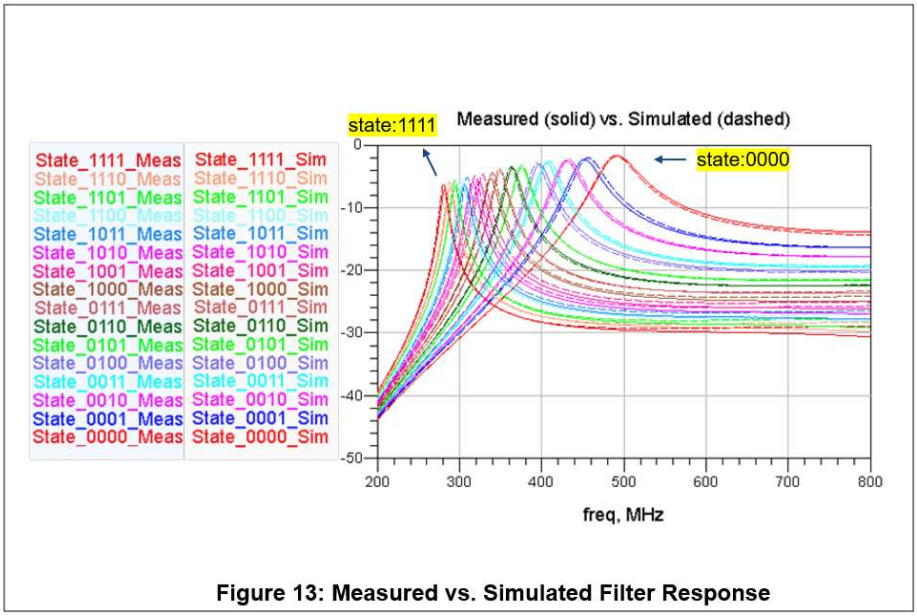


Figure 13: Measured vs. Simulated Filter Response

Note: The simulation was performed using the s-parameter model on p.7 (not the circuit model)

Application Board 2: Tunable Low-Pass Filter 500-1000MHz (2 Switch, 3 element Pi-Network)

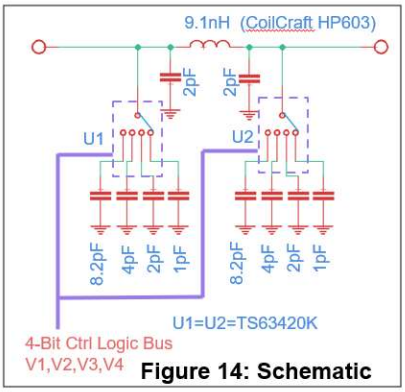


Figure 14: Schematic

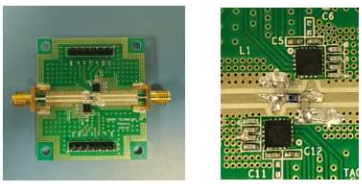


Figure 15: Evaluation Board2

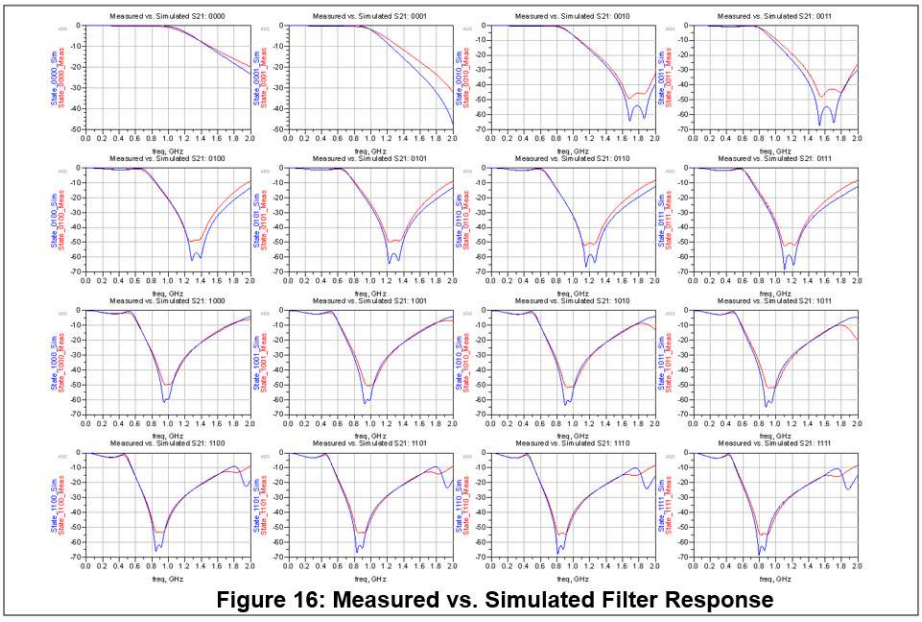


Figure 16: Measured vs. Simulated Filter Response

Note: The simulation was performed using the s-parameter model on p.7 (not the circuit model)

12.0 Standard Tuning Switch Configurations

12.1 Series Configuration

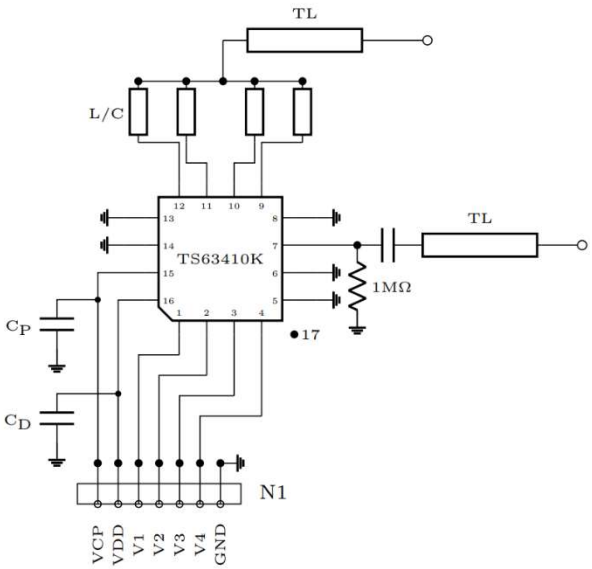


Figure 17. Series configuration. DC reference required.

Note: Series configurations require DC path since all RF and ANT ports are AC coupled. The DC reference can be provided through a 1 MΩ resistor, as shown in Fig. 17.

12.2 Shunt Configuration

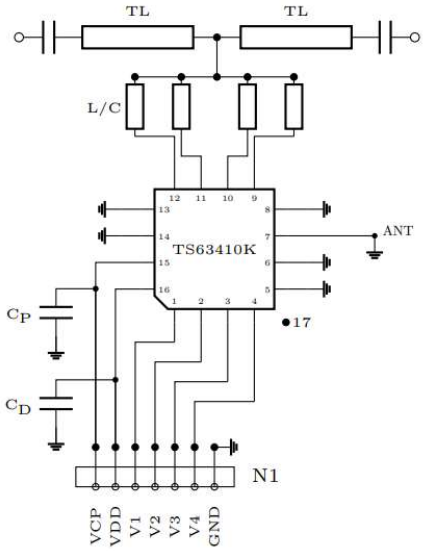


Figure 28. Shunt configuration. No DC reference required.

Note: Shunt configurations do not require DC path to ground since the ANT port is DC grounded, as shown in Fig. 18.

13.0 Device Package Information

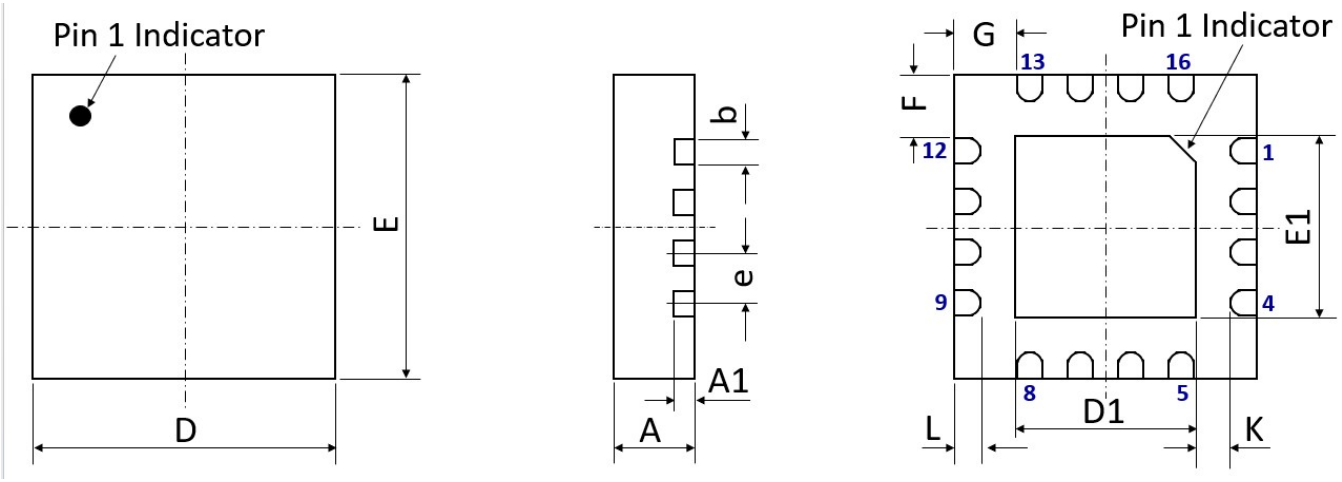


Figure 19 Device Package Drawing
(All dimensions are in mm)

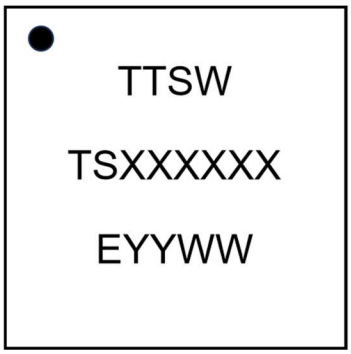
Table 7 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.80	±0.05	E	3.00 BSC	±0.05
A1	0.203	±0.02	E1	1.70	±0.05
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	3.00 BSC	±0.05	G	0.625	±0.05
D1	1.70	±0.05	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

Top-marking specification:



● = Pin 1 indicator
TTSW = Tagore Technology SWitch
TSXXXXXX = Part number (8 digits max)
E = A fixed letter before the date code
YY = Last two digits of assembly year
WW = Assembly work week

14.0 PCB Land Design

Guidelines:
[1] 4 layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 3(X)×3(Y)=9.

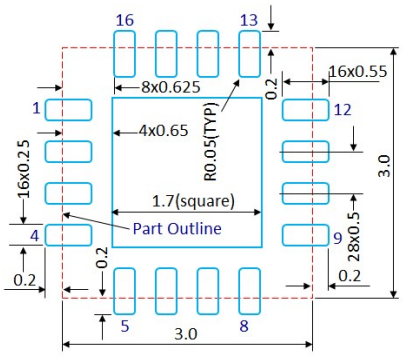
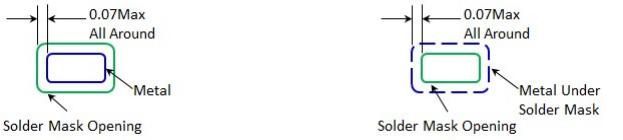


Figure 20 PCB Land Pattern
(Dimensions are in mm)



Non-Solder Mask Defined (Preferred)

Solder Mask Defined

Figure 21 Solder Mask Pattern
(Dimensions are in mm)

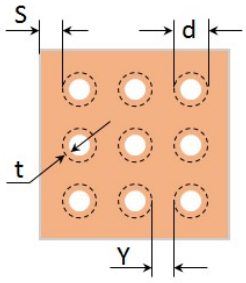


Figure 22 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

15.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125μm.

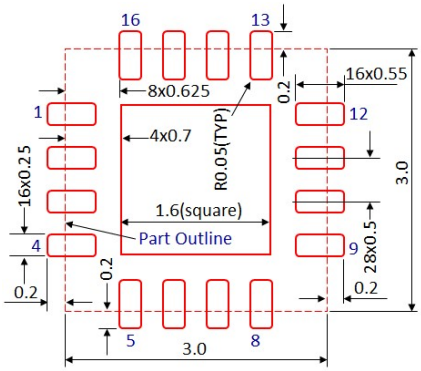


Figure 23 Stencil Openings
(Dimensions are in mm)

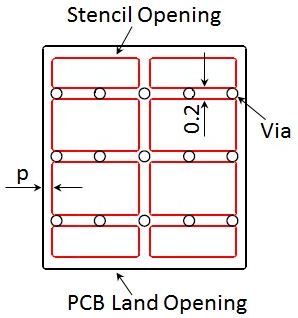


Figure 24 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

16.0 Tape and Reel Information

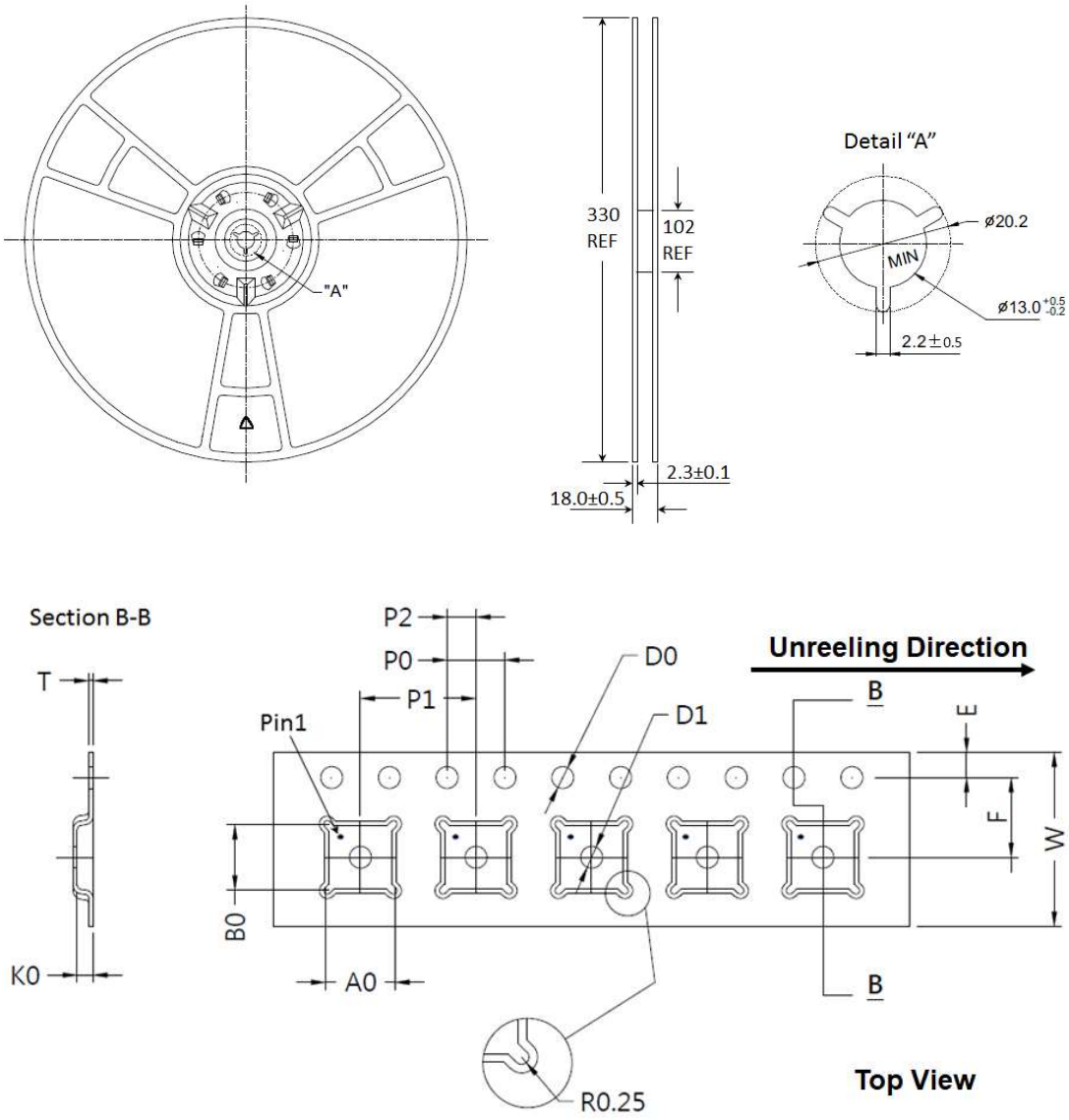


Figure 25 Tape and Reel Drawing

Table 8 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	3.35	±0.10	K0	1.10	±0.10
B0	3.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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