TA9110K – 6 W CW, 30 – 4000 MHz GaN Power Transistor

1.0 Features

- Small signal gain @ 1000 MHz: 17 dB
- Large signal gain @ 1000 MHz: 14 dB
- PSAT @ 1000 MHz: 40 dBm
- PAE @ PSAT @ 1000 MHz: 55%
- 28 – 32 V Typical operations
- Operating frequency: 30 MHz to 4.0 GHz

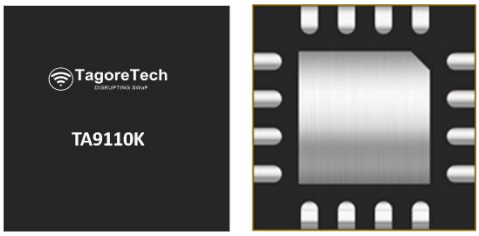


Figure 1.1 Device Image
(16 Pin 3 × 3 × 0.75 mm QFN Package)

2.0 Applications

- Private mobile radio handsets
- Public safety radios
- Cellular infrastructure
- Military radios

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TA9110K is a broadband GaN power transistor capable of delivering 6 W CW from 30 MHz to 4.0 GHz frequency band. The transistor can be used at lower frequencies with reduced output power. The input and output can be matched for best power and efficiency for the desired band.

The TA9110K is packaged in a compact, low-cost Quad Flat No lead (QFN) 3 x 3 x 0.75 mm, 16 leads plastic package.

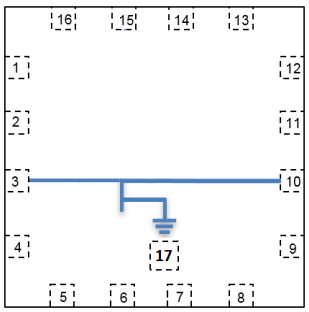


Figure 3.1 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 4.1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TA9110K	16 Pin 3 × 3 × 0.75 mm QFN	Tape and Reel	3000	13” (330 mm)	18 mm	TA9110KMTRPBF
Tuned Evaluation Board, 30 – 2700 MHz						TA9110K-EVB-A
Tuned Evaluation Board, 30 – 512 MHz						TA9110K-EVB-B
Tuned Evaluation Board, 3300 – 3800 MHz						TA9110K-EVB-C
Tuned Evaluation Board, 1500 – 1800 MHz						TA9110K-EVB-D
Tuned Evaluation Board, 30 – 800 MHz						TA9110K-EVB-E
Tuned Evaluation Board, 950 – 1800 MHz						TA9110K-EVB-F
Tuned Evaluation Board, 200 – 2000 MHz						TA9110K-EVB-G

5.0 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Breakdown voltage	V_{DS}	+120	V
Gate voltage	V_{GS}	-10 to +2.0	V
Drain current	I_{DS}	0.75	A
Gate current	I_{GS}	2.1	mA
Power dissipation CW	P_{diss}	12	W
RF input power CW, @1000MHz	RF_{IN}	28	dBm
Storage Temperature Range	T_{st}	-55 to +150	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+225	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	8.9	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1A	250 to <500	V
Charged Device Model (CDM)	Level C1	250 to <500	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:
Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

6.0 Pin Description

Table 6.1 Pin Definition

Pin Number	Pin Name	Description
1,2, 4-9, 11-16	NC	No internal connection, can be connected to ground
3	V_{GG} & RF_{IN}	Gate voltage and RF input
10	V_{DD} & RF_{OUT}	Drain voltage and RF output
17[1]	Paddle/Slug	Ground

Note: [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heatsinking required.

7.0 RF Electrical Specifications

Table 7.1 Electrical Specifications @T_A=+25°C Unless Otherwise Specified;

Parameter	Condition	Minimum	Typical	Maximum	Unit
Small Signal Gain	1000 MHz		17		dB
Large Signal Gain	P_{OUT} = 38 dBm, 1000 MHz		14		dB
P_{SAT}	1000 MHz		40		dBm
Power Added Efficiency (PAE)	P_{OUT} = 38 dBm		46		%
Drain Voltage			32		V
Ruggedness	All phase, P_{OUT} = 38 dBm	VSWR = 10:1			

Note: Data taken from 30 – 2700 MHz broadband reference design (EVB), V_D=+32 V; I_{DQ}=40 mA, CW

8.0 Recommended Operating Conditions

Table 8.1 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltage	V_{DD}	+12	+32	+34	V
Gate Voltage	V_{GG}	-3.0	-2.55	-2.4	V
Drain Bias Current	I_{DQ}		40		mA
Drain Current	I_{DS}		500		mA
Power Dissipation CW [1]	P_{diss} @ 38 dBm Pout			10	W
Operating Temperature Range		-40	+25	+85	°C

Note: [1] @TC = +85°C

9.0 Bias and Sequencing

Table 9.1 Bias and Sequencing

Turn ON Device	Turn OFF Device
1. Set V_G to -5 V 2. Set V_D to +32 V 3. Adjust V_G to reach required I_{DQ} current 4. Apply RF power	1. Turn RF power off 2. Turn off V_D 3. Turn off V_G

10.0 Typical Characteristics

10.1 30 – 2700 MHz EVB A (Vd=32 V, I_{DQ}=40 mA, CW, T_A=+25°C)

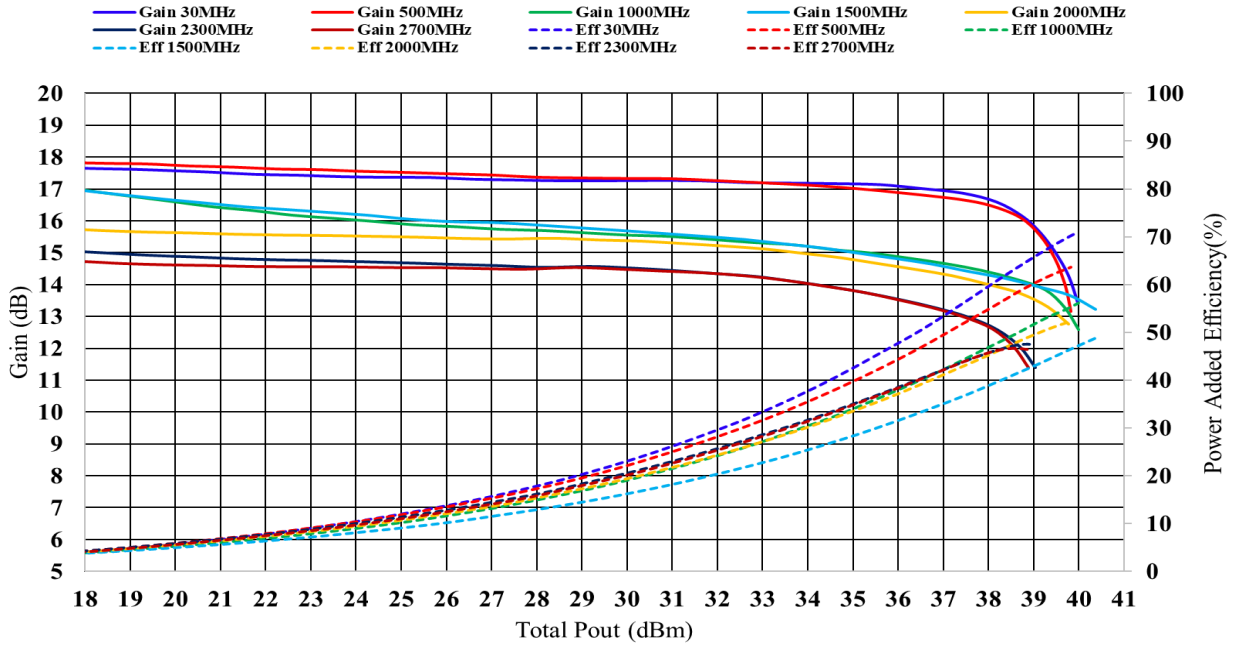


Figure 10.1.1 Gain and PAE vs P_{OUT} (30-2700 MHz)

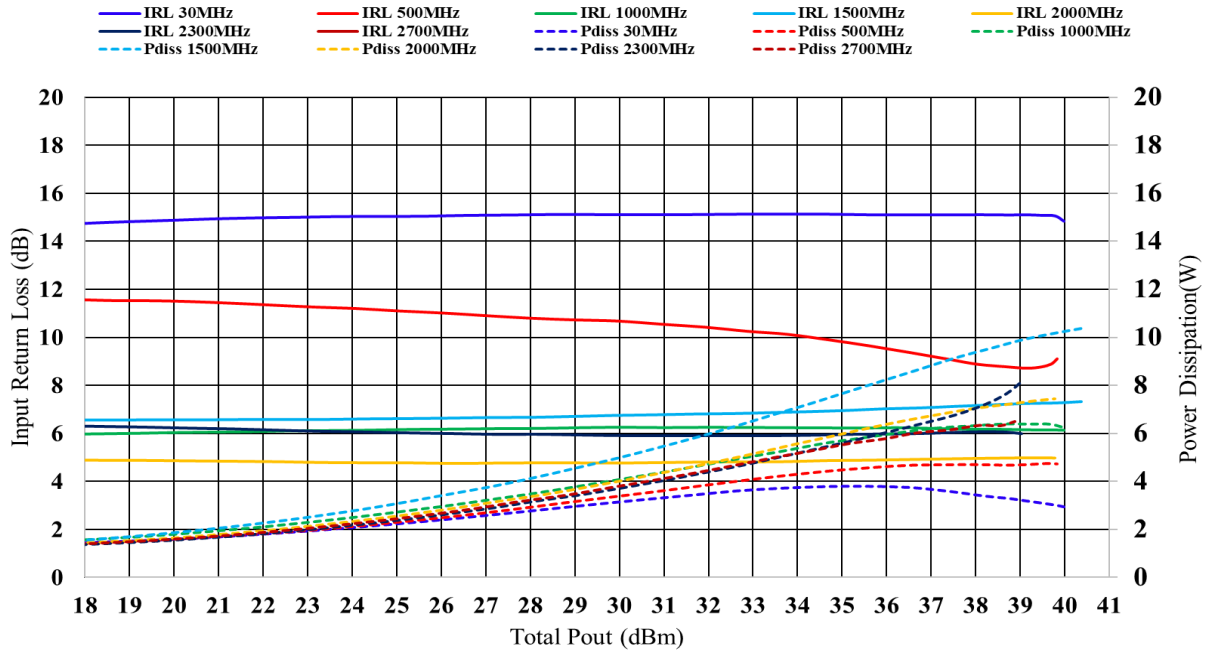


Figure 10.1.2 IRL and P_{diss} vs P_{OUT} (30-2700 MHz)

10.2 30 – 2700 MHz EVB A (Vd=32 V, I_{DQ}=40 mA, LTE, 8 dB PAPR, 4.515 MHz BW, T_A=+25°C)

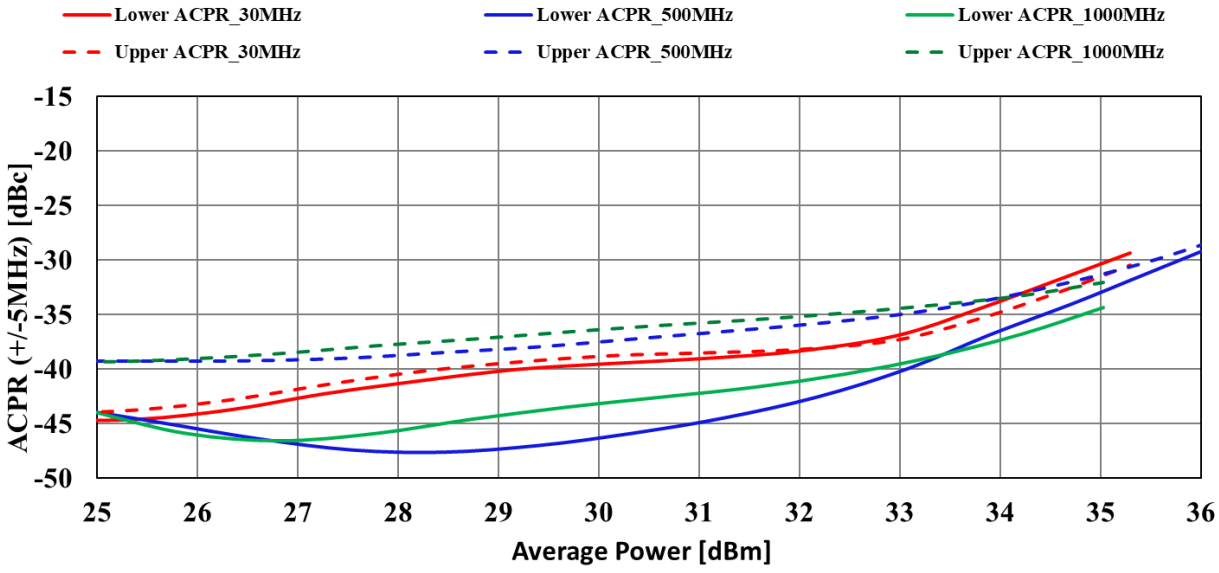


Figure 10.2.1 ACPR vs P_{OUT} (30-1000 MHz)

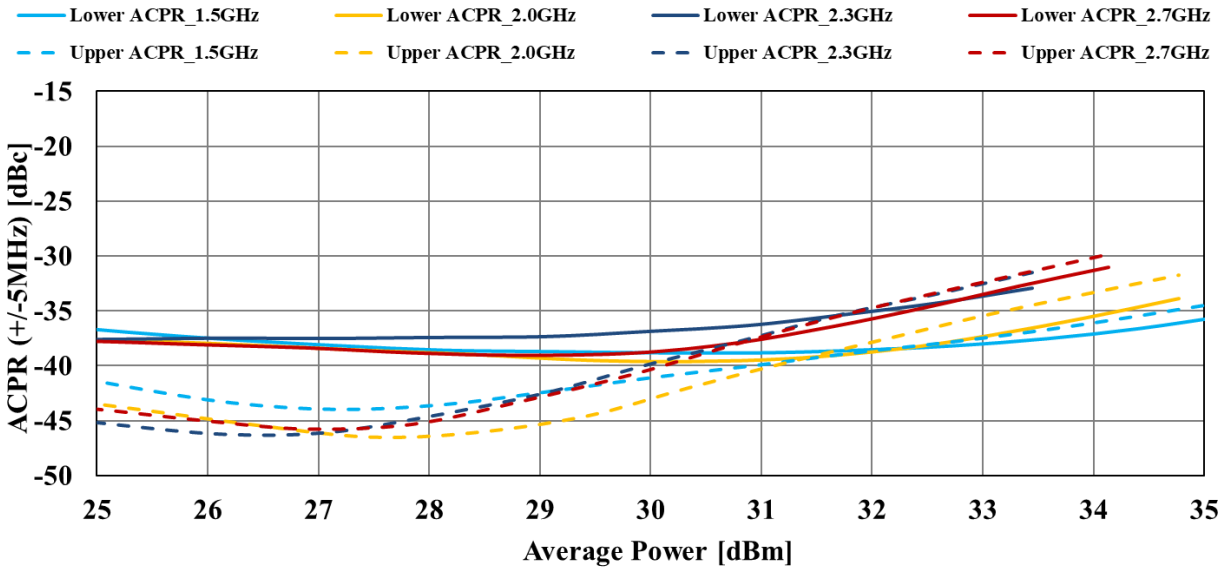


Figure 10.2.2 ACPR vs P_{OUT} (1500-2700 MHz)

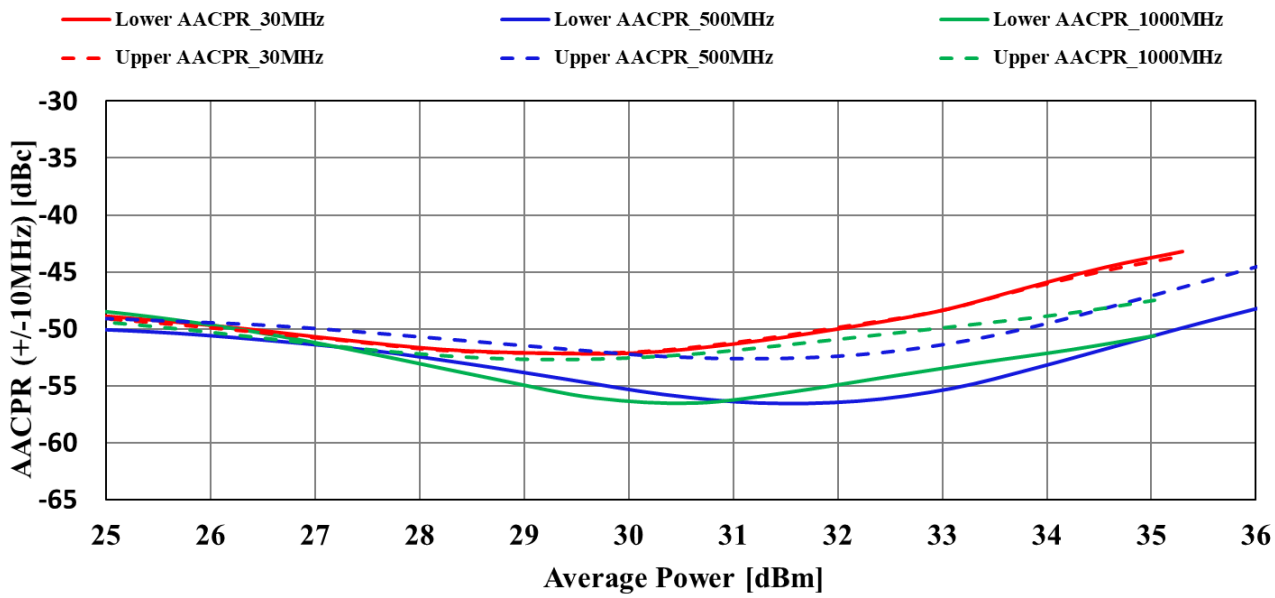


Figure 10.2.3 AACPR vs P_{OUT} (30-1000 MHz)

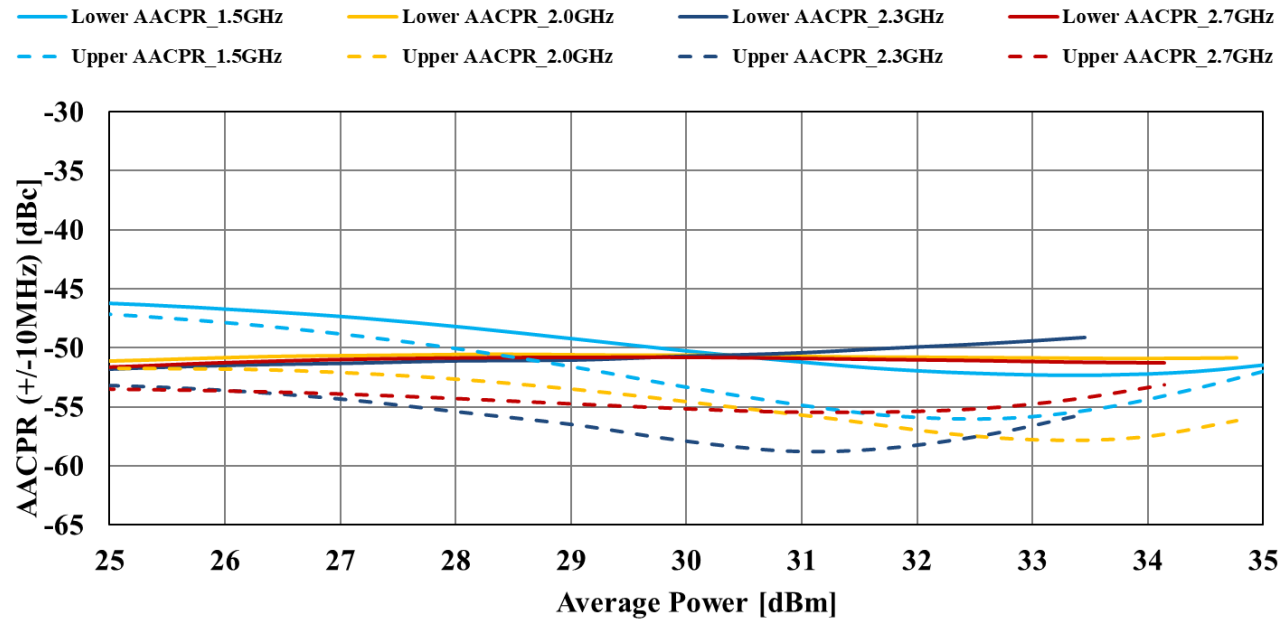


Figure 10.2.4 AACPR vs P_{OUT} (1500-2700 MHz)

10.3 30 – 2700 MHz EVB A (Vd=32 V, I_{DQ}=40 mA, CW, Over Temp -40°C to +85°C)

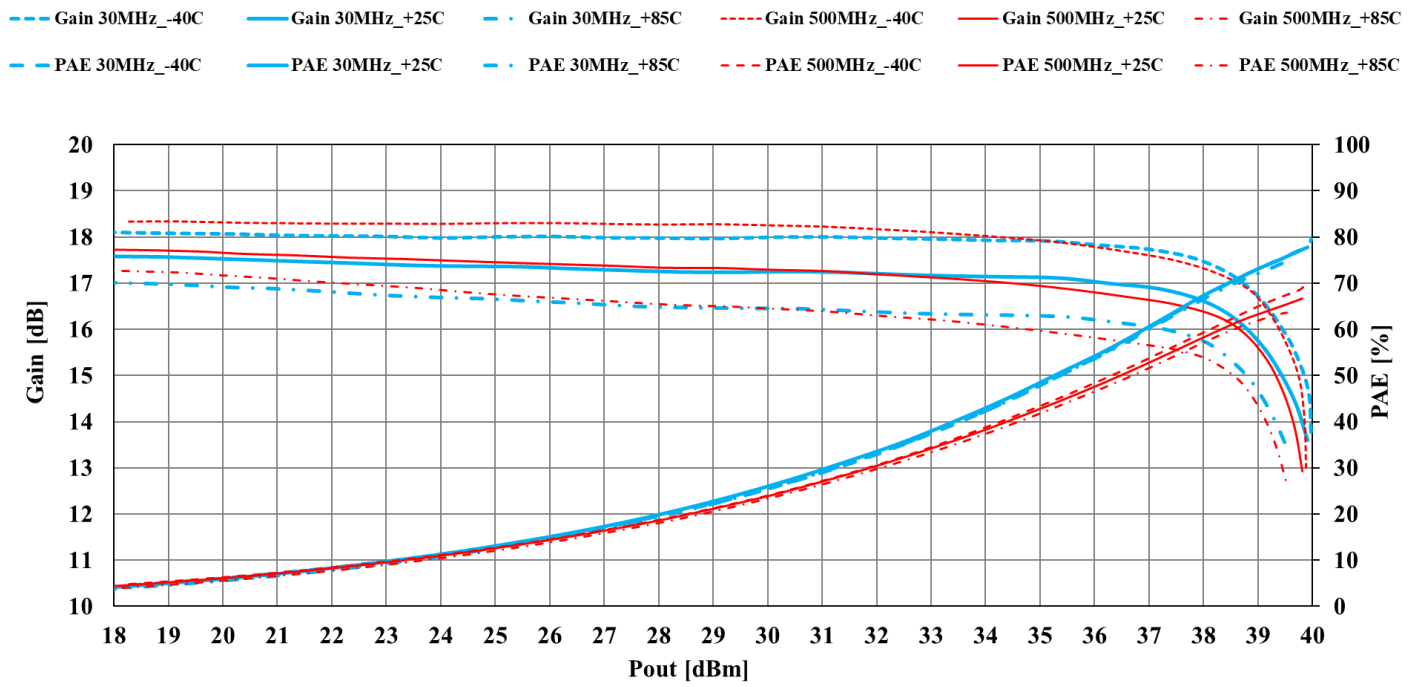


Figure 10.3.1 Gain and PAE vs P_{OUT} (30-500 MHz)

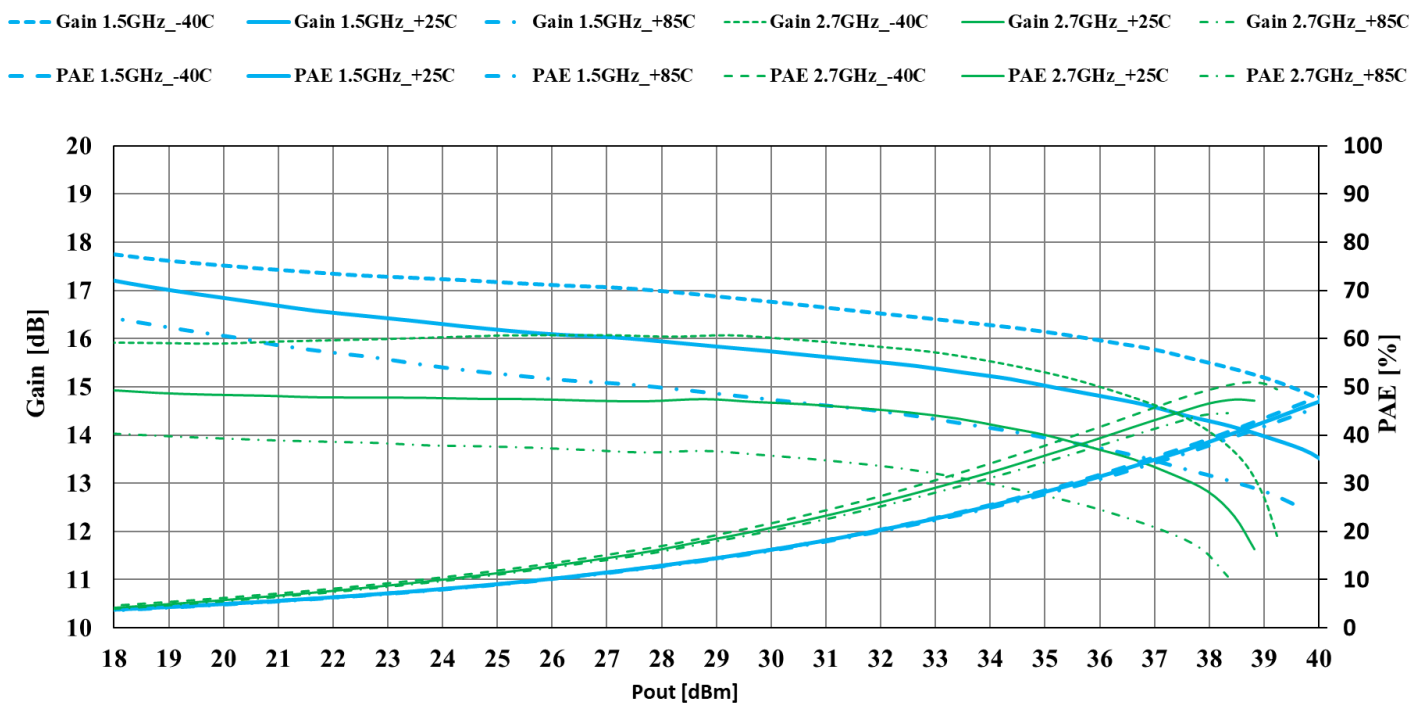


Figure 10.3.2 Gain and PAE vs P_{OUT} (1500-2700 MHz)

11.0 Evaluation Boards

11.1 30 – 2700 MHz EVB A

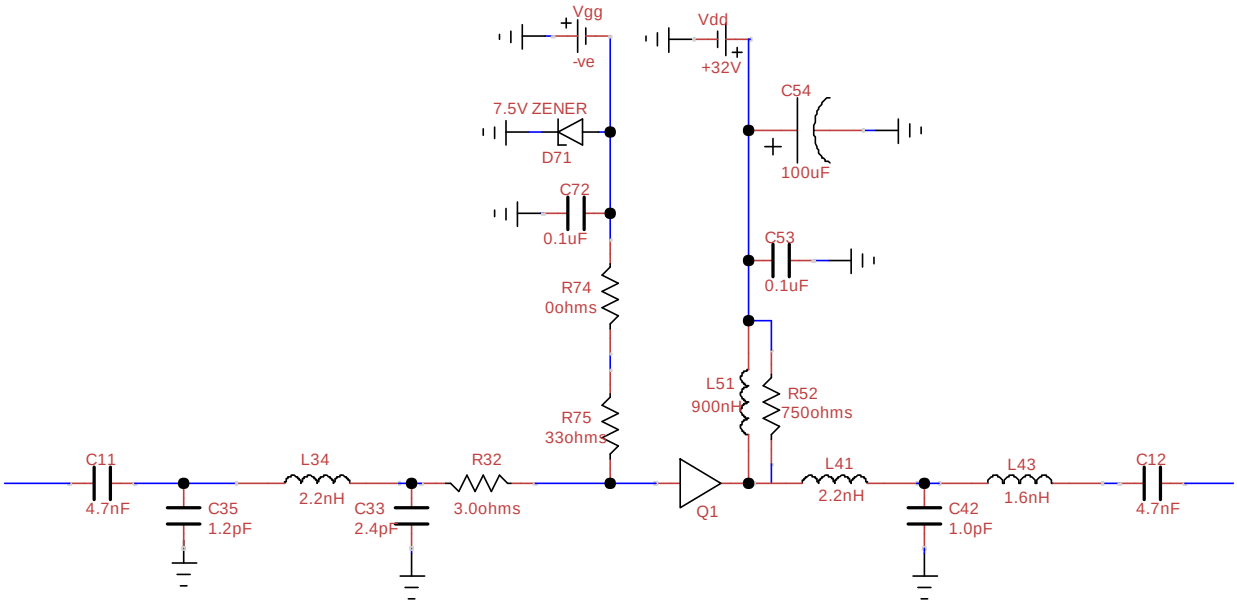
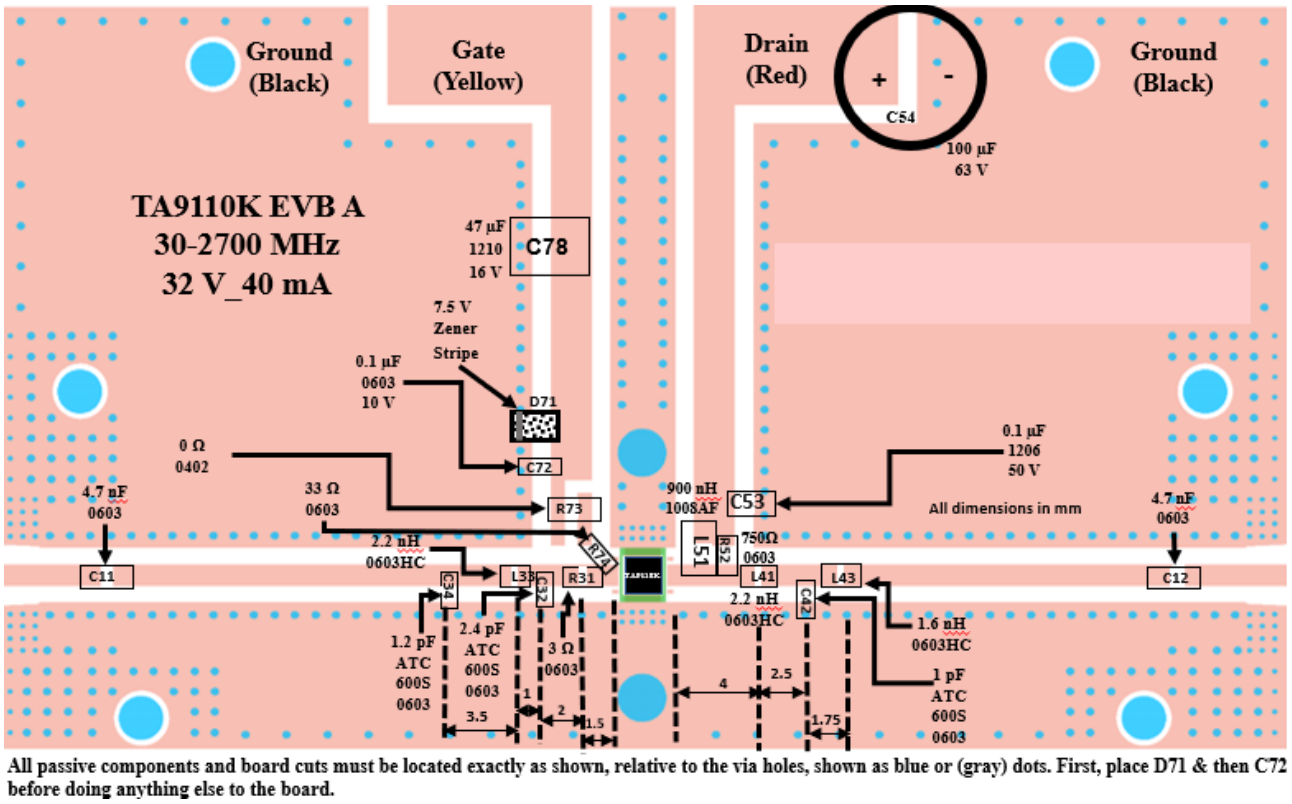


Figure 11.1.1 Schematic of the 30 – 2700 MHz EVB A



All passive components and board cuts must be located exactly as shown, relative to the via holes, shown as blue or (gray) dots. First, place D71 & then C72 before doing anything else to the board.

Figure 11.1.2 Board Layout of the 30 – 2700 MHz EVB A

Table 11.1.1 BOM of the 30 – 2700 MHz EVB A

Component ID	Value	Manufacturer	Recommended Part Number
C11,12	4.7 nF, 50 V	Murata	GRM1885C1H472JA01D
R31	3 Ω	Vishay	RCS06033R00FKEA
C32	2.4 pF	AVX	600S2R4CT250XT
L33, L41	2.2 nH	Coil craft	0402HP-2N2XJE
C34	1.2 pF	AVX	600S1R2CT250XT
C42	1 pF	AVX	600S1R0CT250XT
L43	1.6 nH	Coil craft	0603HC-1N6XGLW
L51	900 nH	Coil craft	1008AF-901XJLC
R52	750 Ω	Vishay	CRCW0603750RFKEB
C53	0.1 µF, 50 V	Murata	GRM31C5C1H104JA01L
C54	100 µF, 63 V	Nichicon	UPW1J101MPD1TD
D71	7.5 V Zener	On Semiconductor	MMSZ5236BT1G
C72	0.1 µF, 10 V	AVX	0603ZC104K4T2A
R73	0 Ω	Vishay	CRCW06030000Z0EAC
R74	33 Ω	ROHM Semiconductor	ESR03EZPJ330
R78	47 µF, 16 V	Murata	GRM32ER61C476ME15L
Q1	6 W GaN Transistor	Tagore Tech	TA9110K
PCB		Rogers RO4350B, 20 mils, 2 oz copper	

Note: Please refer to the application notes on our website for details about the EVBs mentioned above, as well as the additional EVBs listed in Table 4.1.

12.0 Device Package Information

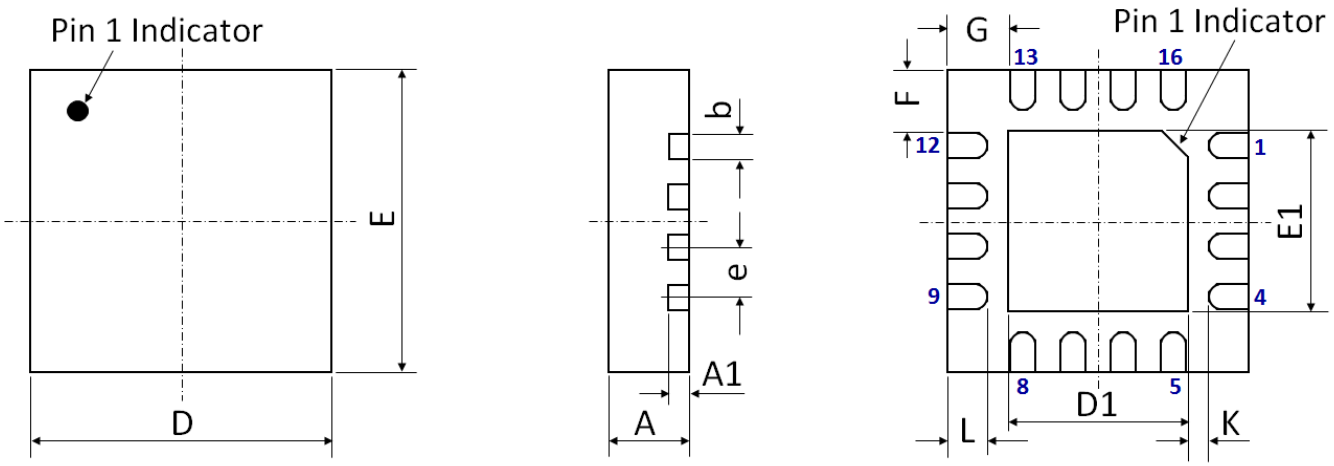


Figure 12.1 Device Package Drawing
(All dimensions are in mm)

Table 12.1 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.750	±0.05	E	3.00 BSC	±0.05
A1	0.203	±0.02	E1	1.70	±0.05
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	3.00 BSC	±0.05	G	0.625	±0.05
D1	1.70	±0.05	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5 µm ~ 20 µm (Typical 10 µm ~ 12 µm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

13.0 PCB Land Design

Guidelines:
[1] 2-layer PCB is recommended
[2] Via diameter is recommended to be 0.3 mm to prevent solder wicking inside the vias
[3] Thermal vias shall only be placed on the center pad and should be filled/plugged with solder or copper
[4] The maximum via number for the center pad is 3(X)×3(Y)=9

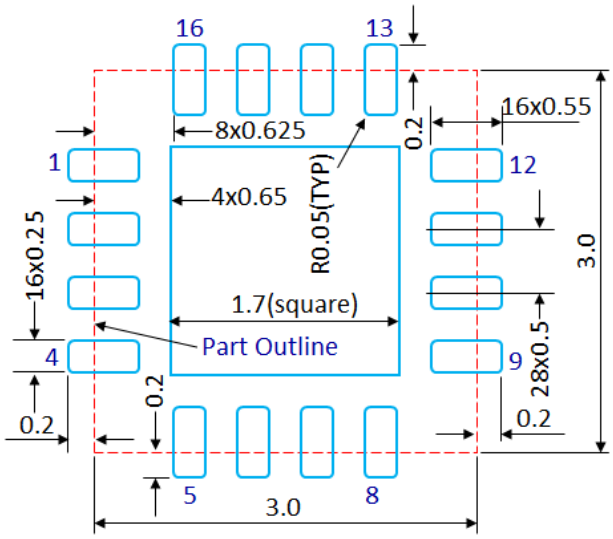


Figure 13.1 PCB Land Pattern
(Dimensions are in mm)

Non-Solder Mask Defined
(Preferred)

Solder Mask Defined

Figure 13.2 Solder Mask Pattern
(Dimensions are in mm)

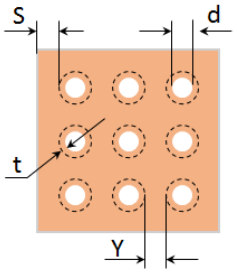


Figure 13.3 Thermal Via Pattern
(Recommended Values: S≥0.15 mm; Y≥0.20 mm; d=0.3 mm; Plating Thickness t=25 µm or 50 µm)

14.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125 μm.

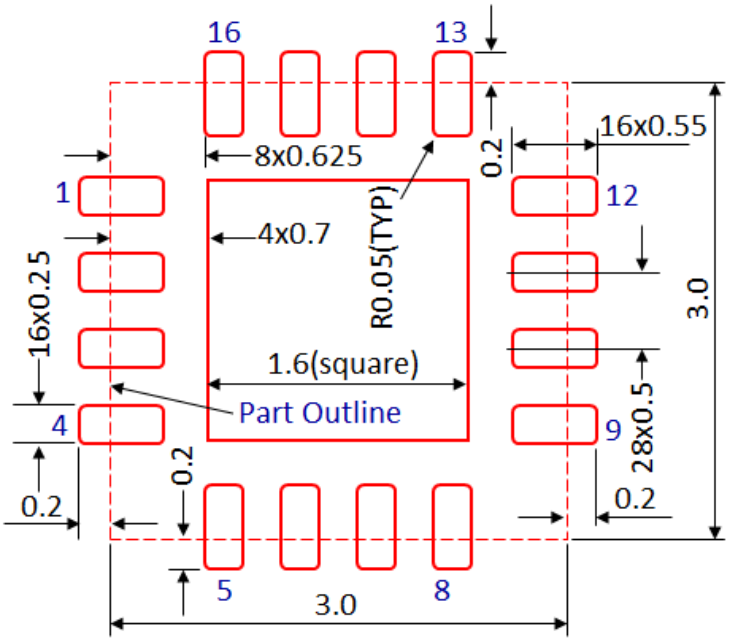


Figure 14.1 Stencil Openings
(Dimensions are in mm)

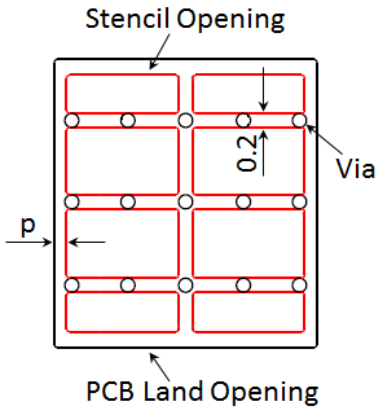


Figure 14.2 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

15.0 Tape and Reel Information

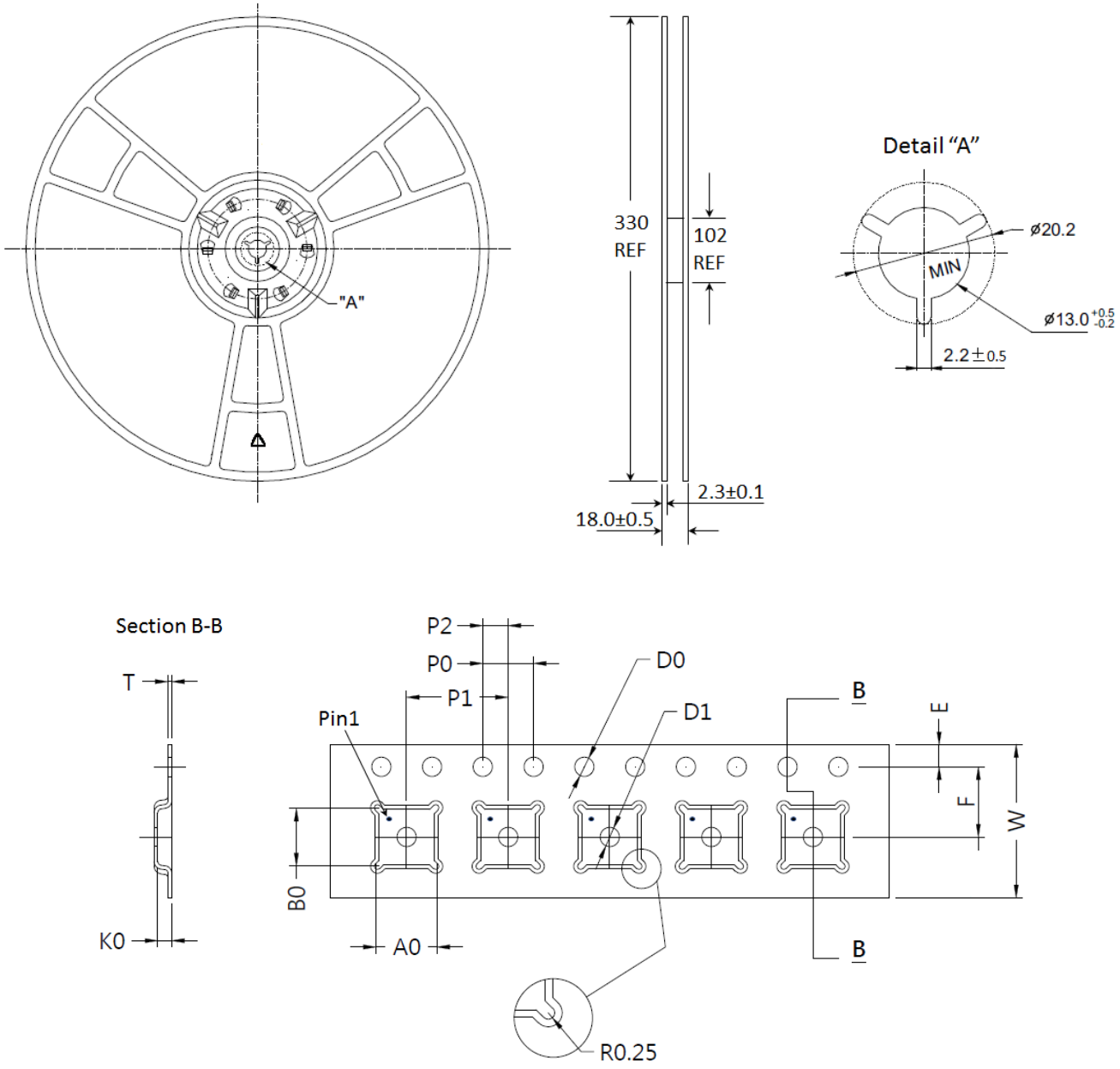


Figure 15.1 Tape and Reel Drawing

Table 15.1 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	3.35	±0.10	K0	1.10	±0.10
B0	3.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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