TA9310E – 20 W CW, 500 – 4000 MHz GaN Power Transistor

1.0 Features

- Small signal gain @ 900 MHz: 17.5 dB
- Large signal gain @ 900 MHz: 14.0 dB
- PSAT @ 900 MHz: 44 dBm
- PAE @ PSAT @ 900 MHz: >55%
- 28 – 32 V Typical operation
- Operating frequency: 30 MHz to 4.0 GHz

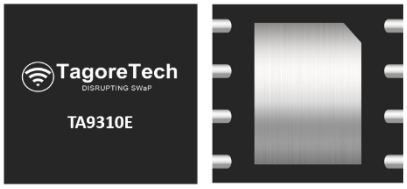


Figure 1.1 Device Image
(8 Pin 5 × 6 × 0.75 mm DFN Package)

RoHS/REACH/Halogen Free Compliance

2.0 Applications

- Private mobile radio handsets
- Public safety radios
- Cellular infrastructure
- Military radios

3.0 Description

The TA9310E is a broadband GaN power transistor capable of delivering 20 W CW from 500 MHz to 4.0 GHz frequency band. The transistor can be used at lower frequencies with reduced output power. The input and output can be matched for best power and efficiency for the desired band.

The TA9310E is packaged in a compact, low-cost Dual Flat No lead (DFN) 5 x 6 x 0.75 mm, 8 leads plastic package.

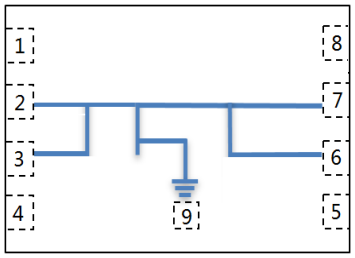


Figure 3.1 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 4.1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TA9310E	8 Pin 5 × 6 × 0.75 mm DFN	Tape and Reel	3000	13” (330 mm)	18 mm	TA9310EMTRPBF
Tuned Evaluation Board, 500 – 2700 MHz						TA9310E-EVB-A
Tuned Evaluation Board, 950 – 1250 MHz						TA9310E-EVB-B
Tuned Evaluation Board, 1500 – 1800 MHz						TA9310E-EVB-C
Tuned Evaluation Board, 2100 – 2500 MHz						TA9310E-EVB-D
Tuned Evaluation Board, 2200 – 2400 MHz						TA9310E-EVB-E

Tuned Evaluation Board, 950 – 1800 MHz	TA9310E-EVB-F
Tuned Evaluation Board, 2700 – 3500 MHz	TA9310E-EVB-G
Tuned Evaluation Board, 300 – 500 MHz	TA9310E-EVB-H
Tuned Evaluation Board, 30 – 48 MHz	TA9310E+TS8441L-EVB-I RF1
Tuned Evaluation Board, 48 – 78 MHz	TA9310E+TS8441L-EVB-I RF2
Tuned Evaluation Board, 78 – 125 MHz	TA9310E+TS8441L-EVB-I RF3
Tuned Evaluation Board, 125 – 200 MHz	TA9310E+TS8441L-EVB-I RF4
Tuned Evaluation Board, 200 – 320 MHz	TA9310E+TS8441L-EVB-I RF5
Tuned Evaluation Board, 320 – 520 MHz	TA9310E+TS8441L-EVB-I RF6
Tuned Evaluation Board, 30 – 512 MHz	TA9310E-EVB-J

5.0 Pin Description

Table 5.1 Pin Definition

Pin Number	Pin Name	Description
1, 4, 5, 8	NC	No internal connection
2, 3	V_{GG} & RF_{IN}	Gate voltage and RF input
6, 7	V_{DD} & RF_{OUT}	Drain voltage and RF output
9[1]	Paddle/Slug	Ground

Note: [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heat sinking required.

6.0 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Breakdown voltage	V_{DS}	+120	V
Gate voltage	V_{GS}	-10 to +2.0	V
Drain current	I_{DS}	3.0	A
Gate current	I_{GS}	7	mA
Power dissipation CW	P_{diss}	28	W
RF input power CW, @900MHz	RF_{IN}	34	dBm
Storage Temperature Range	T_{st}	-55 to +150	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+225	°C

Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	4.9	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1A	250 to <500	V
Charged Device Model (CDM)	Level C1	250 to <500	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:
Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 RF Electrical Specifications

Table 7.1 Electrical Specifications @T_A=+25°C Unless Otherwise Specified.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Small Signal Gain	900 MHz		17.5		dB
Large Signal Gain	P_{OUT} = 43 dBm, 900 MHz		14.5		dB
P_{SAT}	900 MHz		44		dBm
Power Added Efficiency (PAE)	P_{OUT} = 43 dBm		52		%
Drain Voltage			32	34	V
Ruggedness	All phase, P_{OUT} = 43 dBm	VSWR = 8:1			

Note: Data taken from 500 – 2700 MHz broadband reference design (EVB), V_D=+32 V; I_{DQ}=100 mA, CW

8.0 Recommended Operating Conditions

Table 8.1 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltage	V_{DD}	+12	+32	+34	V
Gate Voltage	V_{GG}	-2.7	-2.58	-2.3	V
Drain Bias Current	I_{DQ}		100		mA
Drain Current	I_{DS}		1200		mA
Power Dissipation CW [1]	P_{diss}			25	W
Operating Temperature Range		-40	+25	+85	°C

Note: [1] @TC = +85°C

9.0 Bias and Sequencing

Table 9.1 Bias and Sequencing

Turn ON Device	Turn OFF Device
1. Set V_G to -5 V 2. Set V_D to +32 V 3. Adjust V_G to reach required I_{DQ} current 4. Apply RF power	1. Turn RF power off 2. Turn off V_D 3. Turn off V_G

10.0 Typical Characteristics

10.1 500 – 2700 MHz EVB A

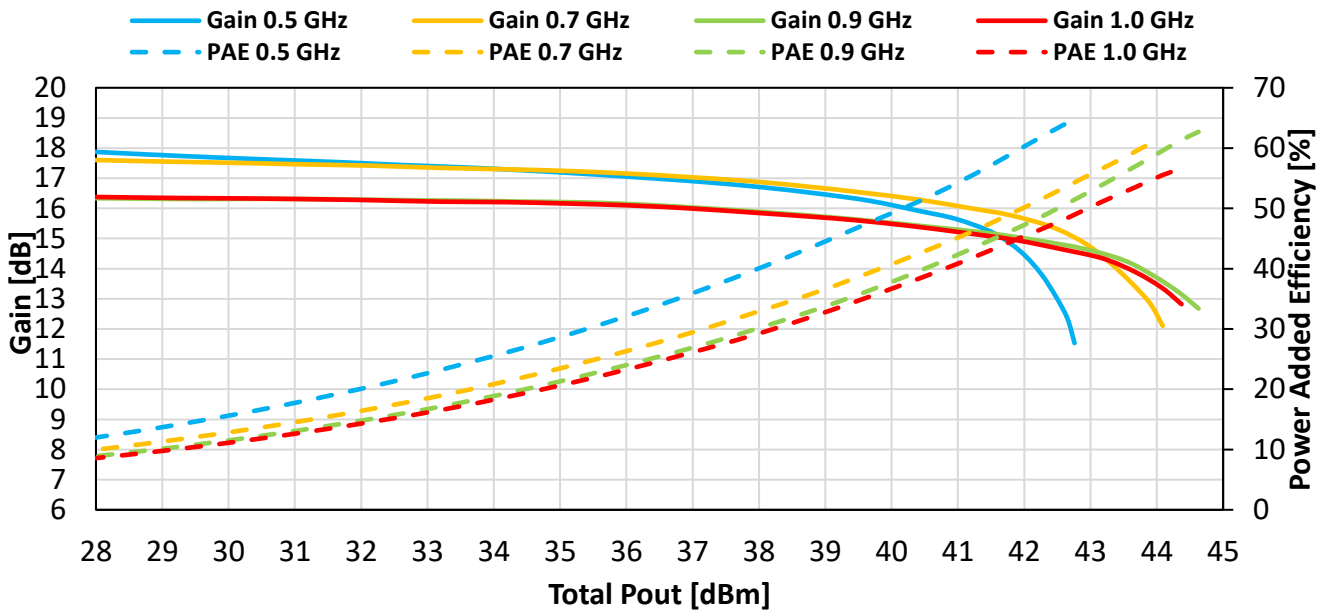


Figure 10.1.1 Gain and PAE vs P_{OUT} (500-1000 MHz)
(V_D=32 V, I_{DQ}=100 mA, CW, T_A=+25°C)

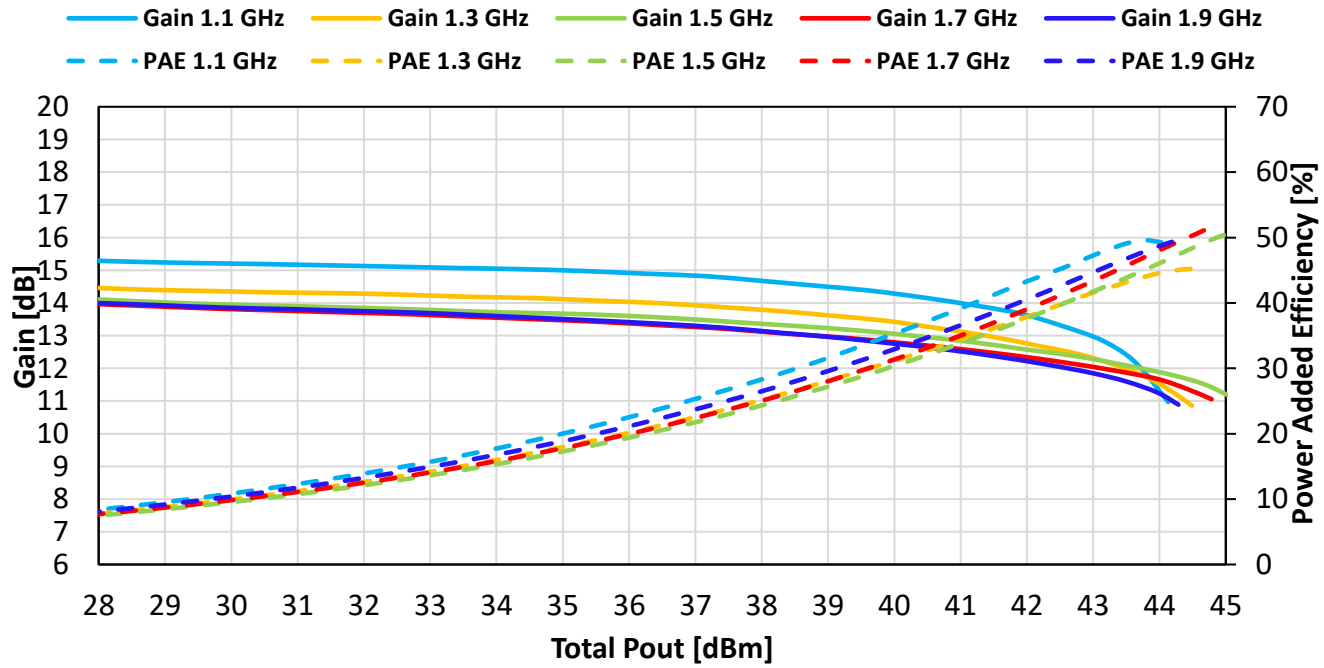


Figure 10.1.2 Gain and PAE vs P_{OUT} (1100-1700 MHz)
(V_D=32 V, I_{DQ}=100 mA, CW, T_A=+25°C)

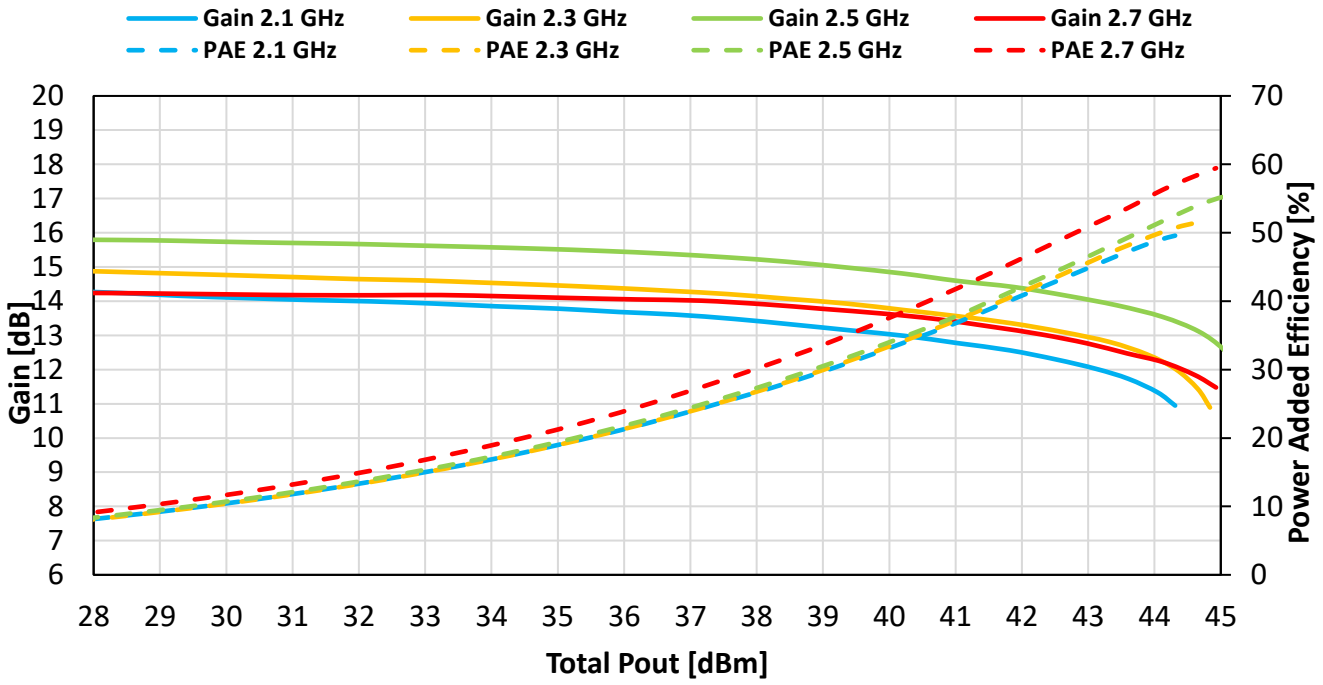


Figure 10.1.3 Gain and PAE vs P_{OUT} (2100-2700 MHz)
(V_D=32 V, I_{DQ}=100 mA, CW, T_A=+25°C)

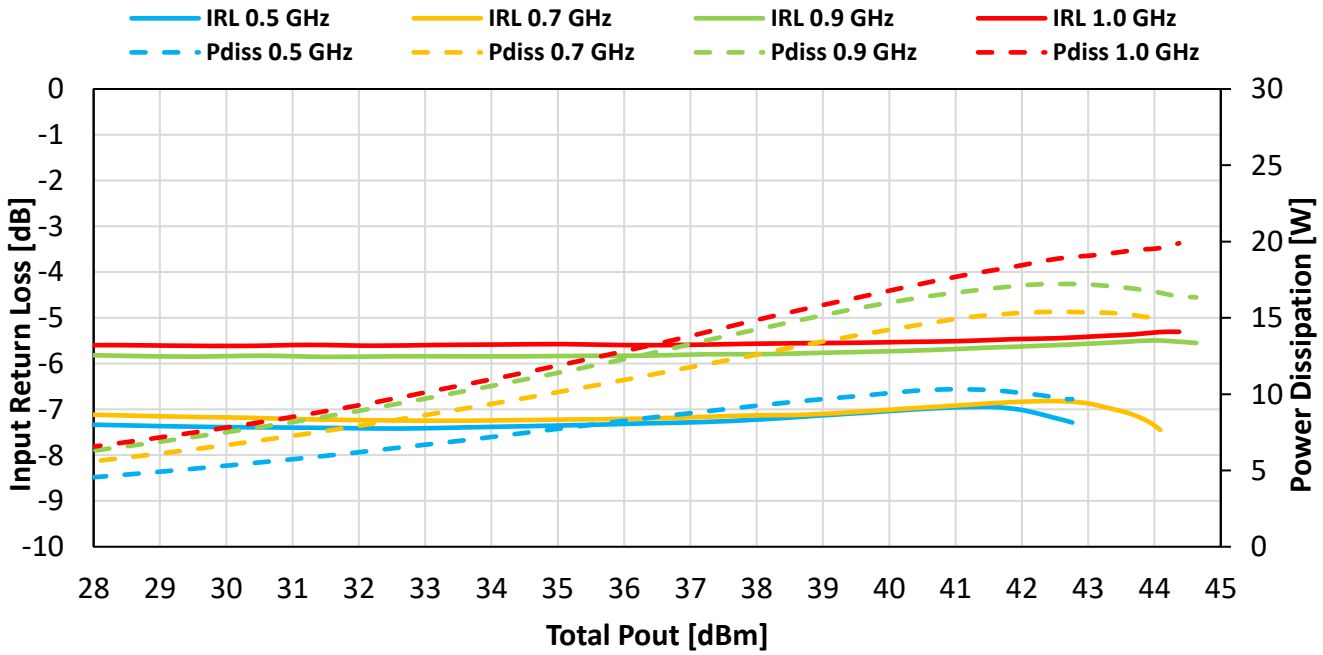


Figure 10.1.4 IRL and P_{diss} vs P_{OUT} (500-1000 MHz)
(V_D=32 V, I_{DQ}=100 mA, CW, T_A=+25°C)

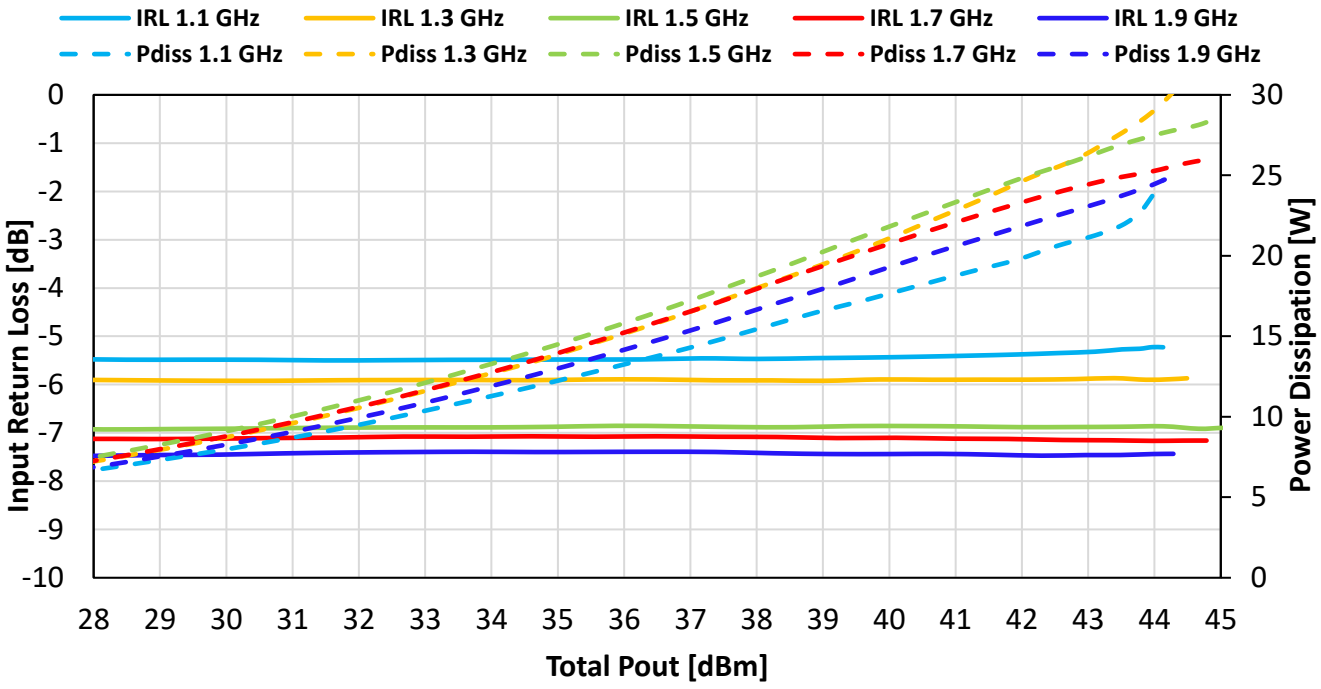


Figure 10.1.5 IRL and P_{diss} vs P_{OUT} (1100-1900 MHz)
(V_D=32 V, I_{DQ}=100 mA, CW, T_A=+25°C)

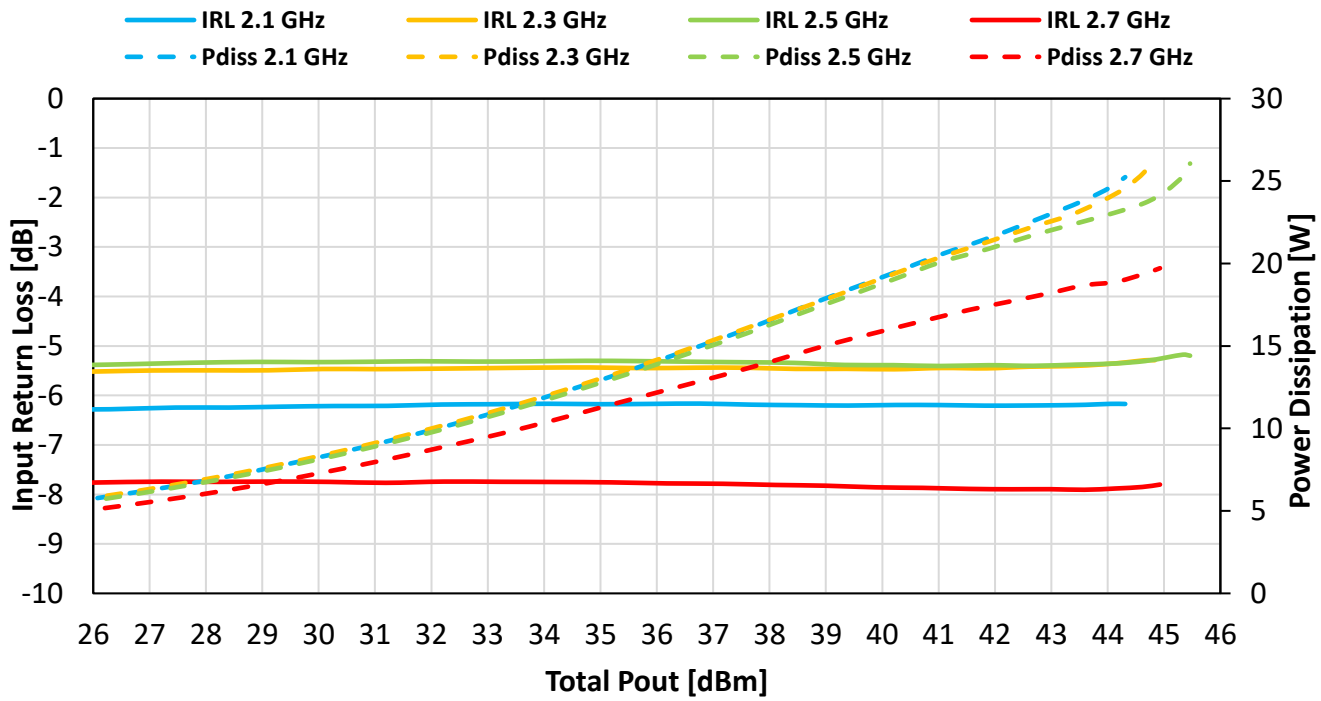


Figure 10.1.6 IRL and P_{diss} vs P_{OUT} (2100-2700 MHz)
(V_D=32 V, I_{DQ}=100 mA, CW, T_A=+25°C)

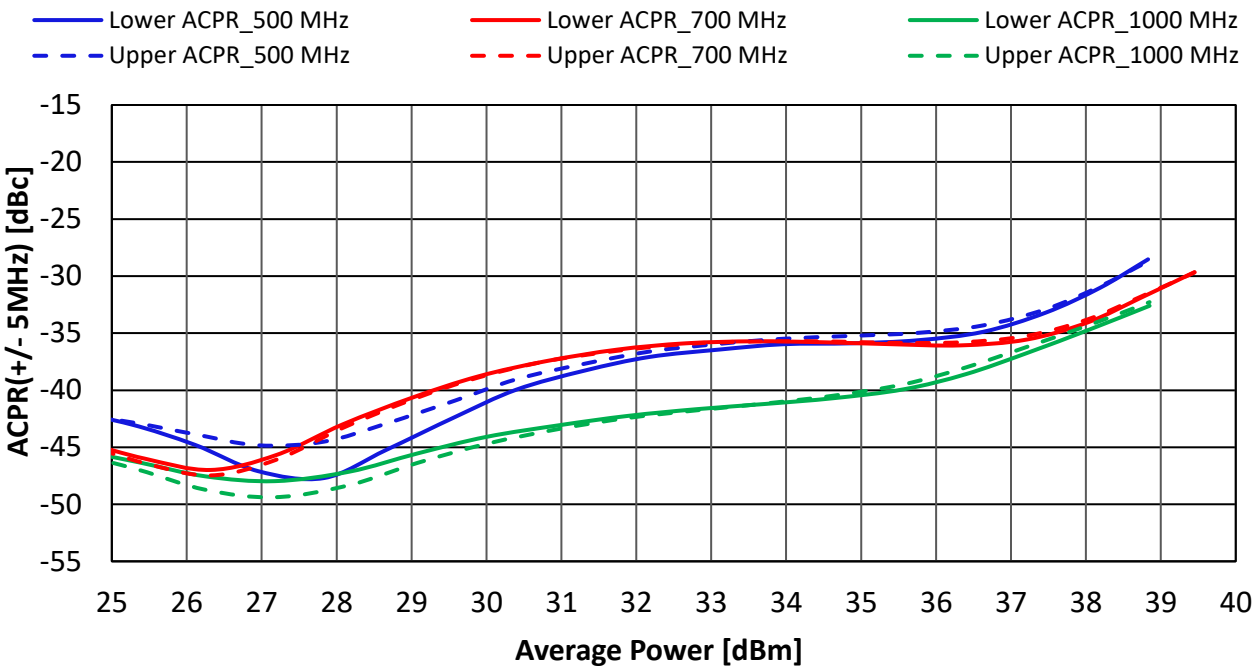


Figure10.1.7 ACPR vs P_{OUT} (500-1000 MHz)
(V_D=32 V, I_{DQ}=100 mA, 8 dB PAPR, 4.515 MHz BW, T_A=+25°C)

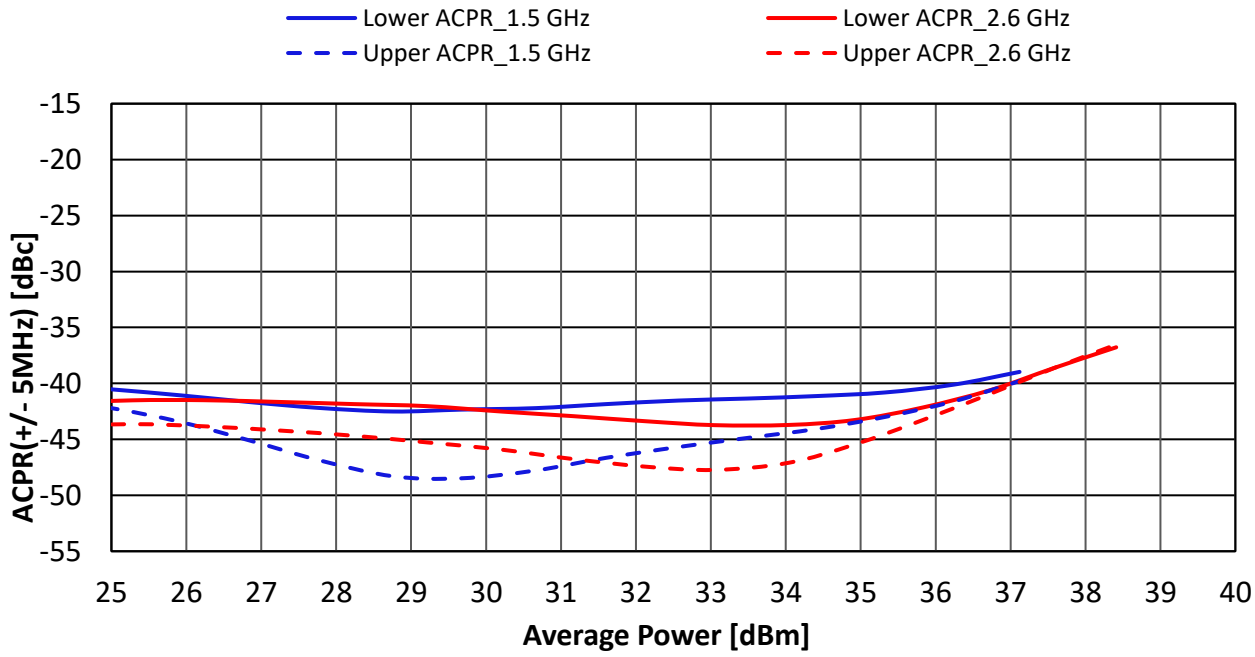


Figure 10.1.8 ACPR vs P_{OUT} (1500-2700 MHz)
(V_D=32 V, I_{DQ}=100 mA, 8 dB PAPR, 4.515 MHz BW, T_A=+25°C)

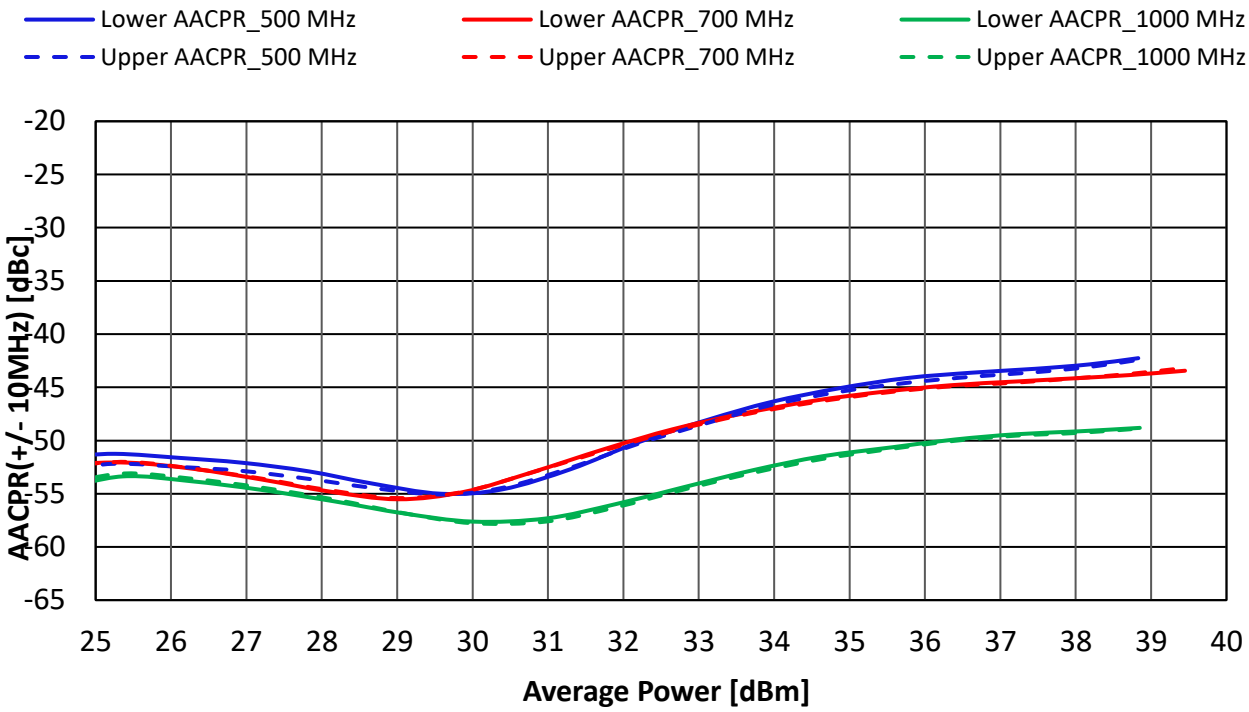


Figure 10.1.9 AACPR vs P_{OUT} (500-1000 MHz)
(V_D=32 V, I_{DQ}=100 mA, 8 dB PAPR, 4.515 MHz BW, T_A=+25°C)

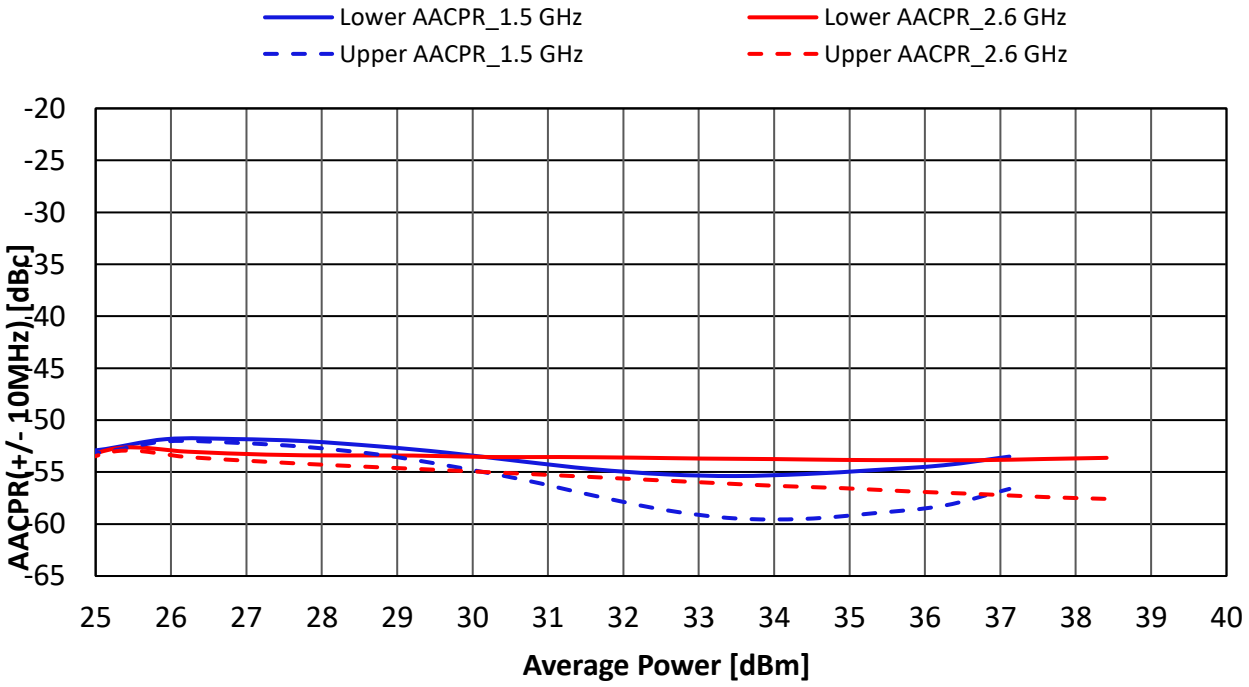


Figure 10.1.10 AACPR vs P_{OUT} (1500-2700 MHz)
(V_D=32 V, I_{DQ}=100 mA, 8 dB PAPR, 4.515 MHz BW, T_A=+25°C)

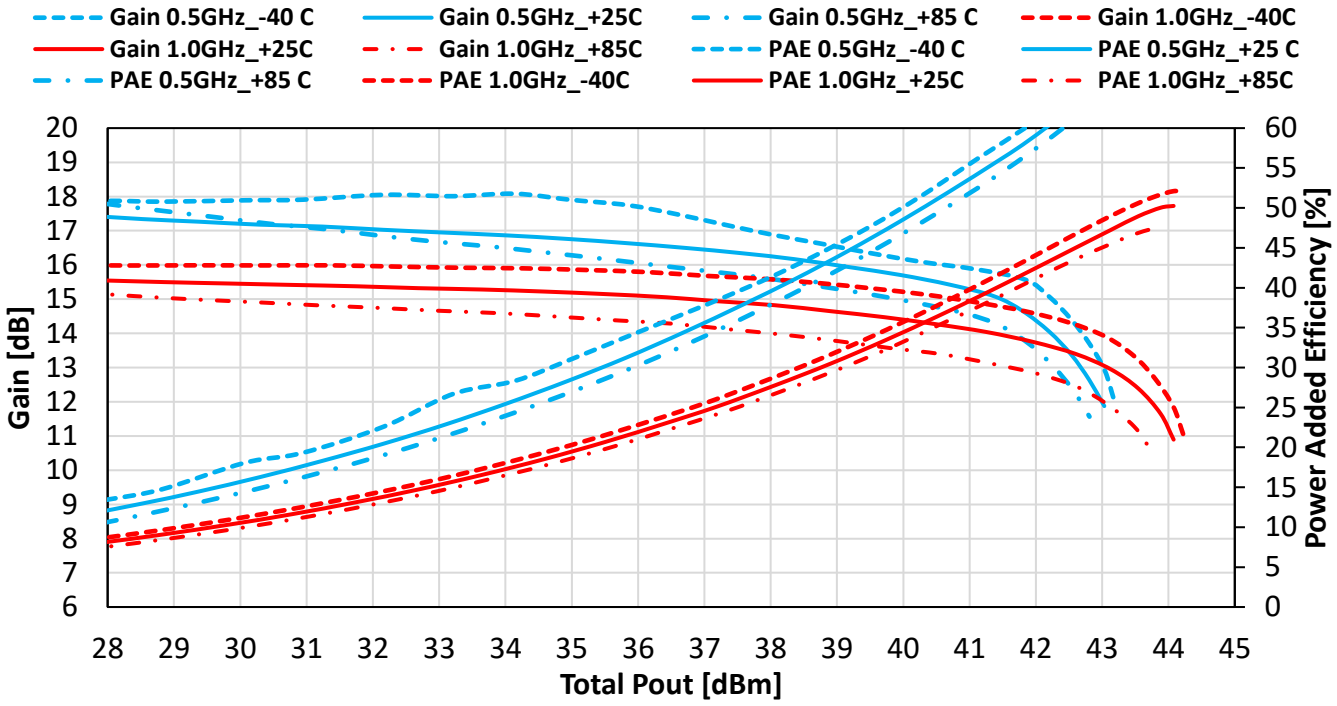


Figure 10.1.11 Gain and PAE vs P_{OUT} (500-1000 MHz) over Temperature
(V_D=32 V, I_{DQ}=100 mA, CW, T_A=+25°C)

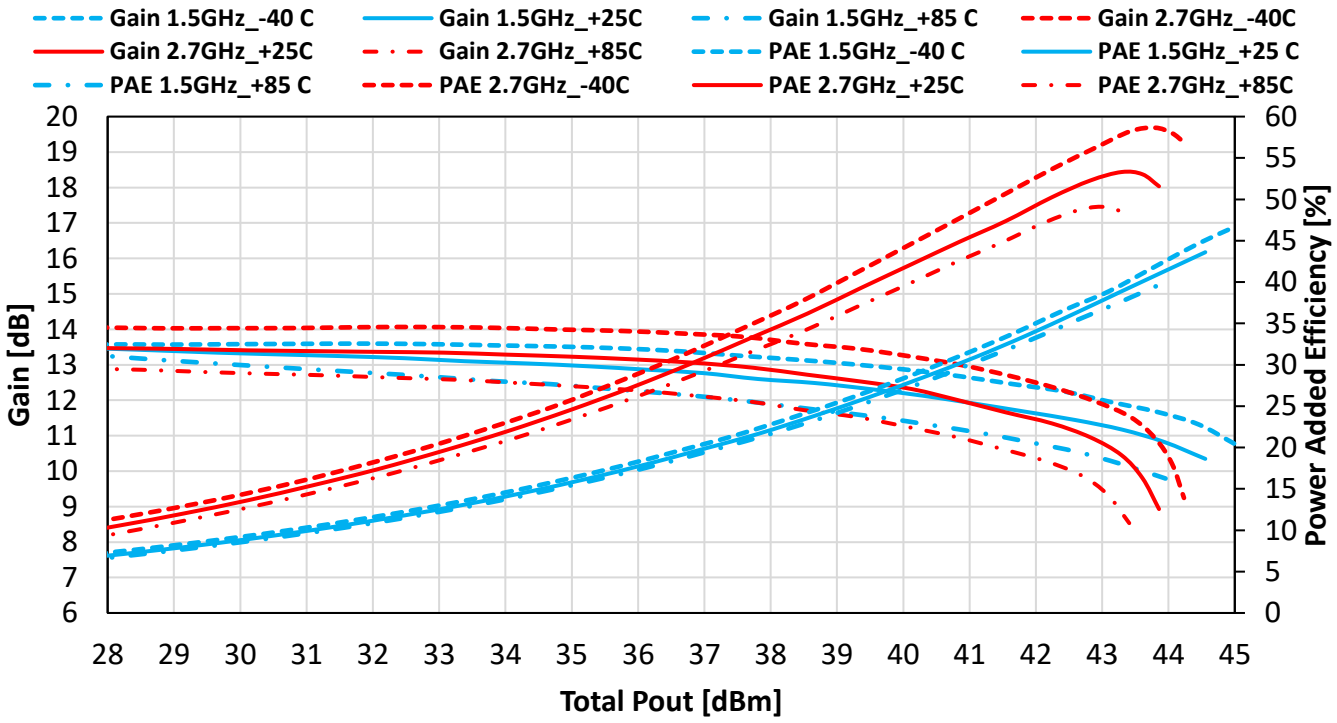


Figure 10.1.12 Gain and PAE vs P_{OUT} (1500-2700 MHz) over Temperature
(V_D=32 V, I_{DQ}=100 mA, CW, T_A=+25°C)

11.0 Evaluation Boards

11.1 500 – 2700 MHz EVB A

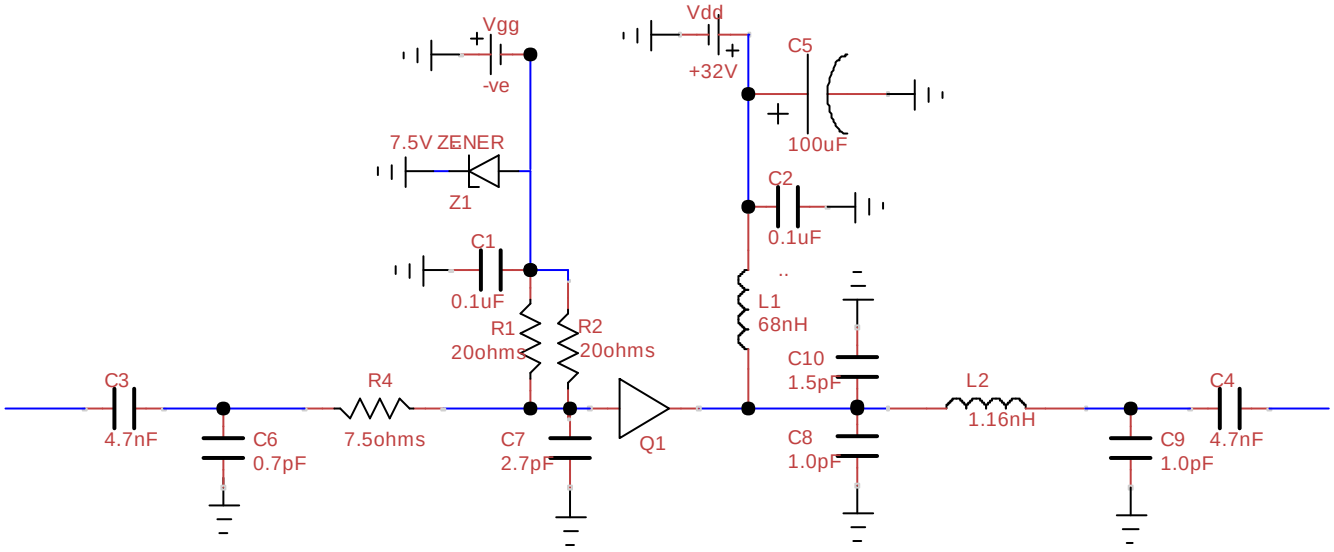
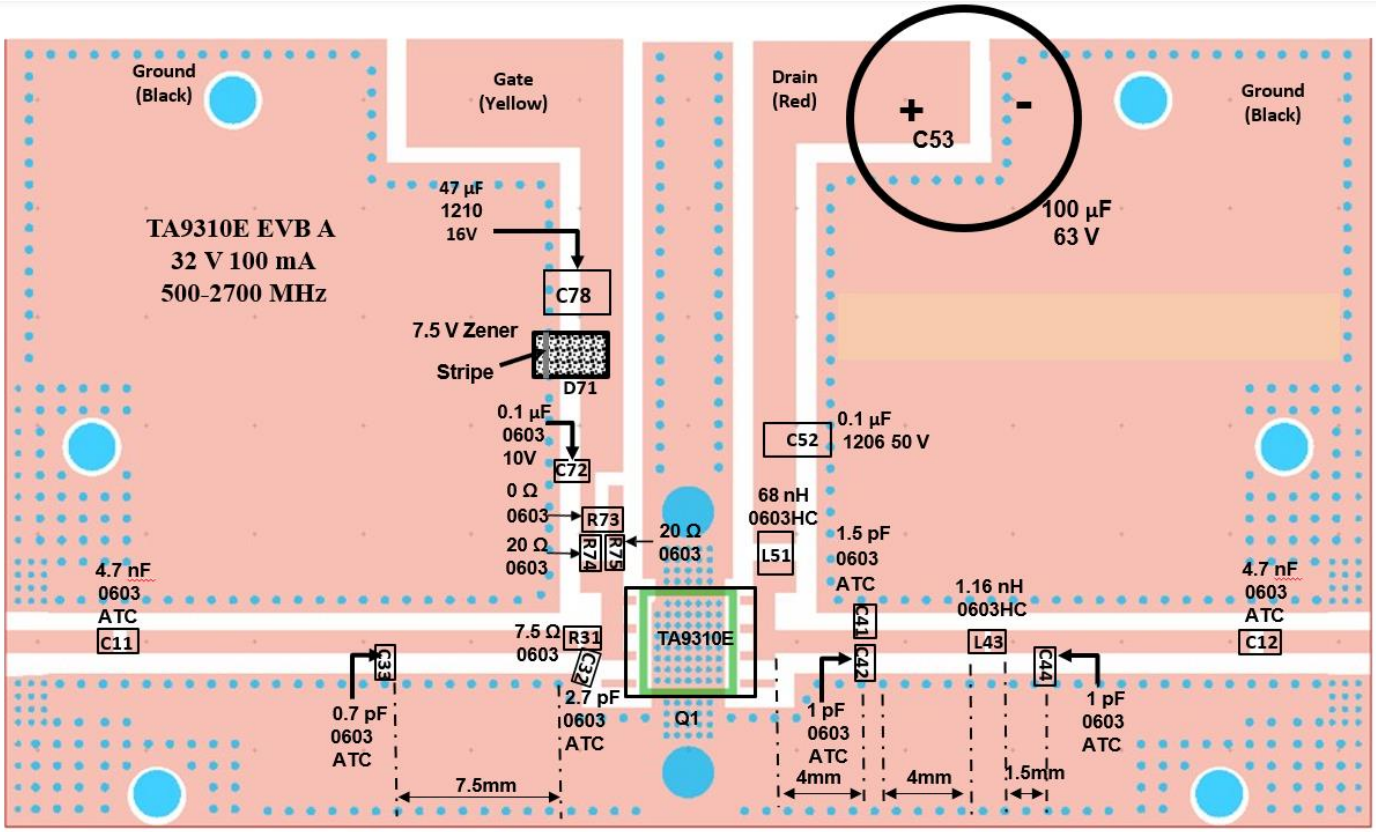


Figure 11.1.1 Schematic of the 500 – 2700 MHz EVB A



Note: Pins 4 and 5 can be grounded

Figure 11.1.2 Board Layout of the 500 – 2700 MHz EVB

Table 11.1.1 BOM of the 500 – 2700 MHz EVB

Component ID	Value	Manufacturer	Recommended Part Number
C3, C4	4.7 nF, 50 V	Murata	GRM1885C1H472JA01
C6	0.7 pF	ATC	600S0R7CT250XT
L2	1.16 nH	Coil craft	0604HQ-1N1XJLC
L1	68n H	Coil craft	1008HQ-68NXGLC
C7	2.7 pF	ATC	600S2R7CT250XT
C10	1.5 pF	ATC	600S1R5CT250XT
C8	1.0 pF	ATC	600S1R0CT250XT
C9	1.0 pF	ATC	600S1R0CT250XT
C1	0.1 µF, 10 V	AVX	0603ZC104K4T2A
C2	0.1 µF, 50 V	Murata	GRM31C5C1H104JA01L
C5	100 µF	Nichicon	UPW1J101MPD1TD
R4	7.5 Ω	Panasonic	ERJ-3RQF7R5V
R3	0 Ω	Panasonic	ERJ-2GE0R00X
R1, R2	20 Ω, 250 mW	Panasonic	ERJ-PA3F20R0V
Z1	7.5 V Zener	On Semiconductor	SZMMSZ5236BT 1G
Q1	20 W GaN Transistor	Tagore Tech	TA9310E
PCB	Rogers RO4350B, 20 mils, 2 oz copper		

12.0 Device Package Information

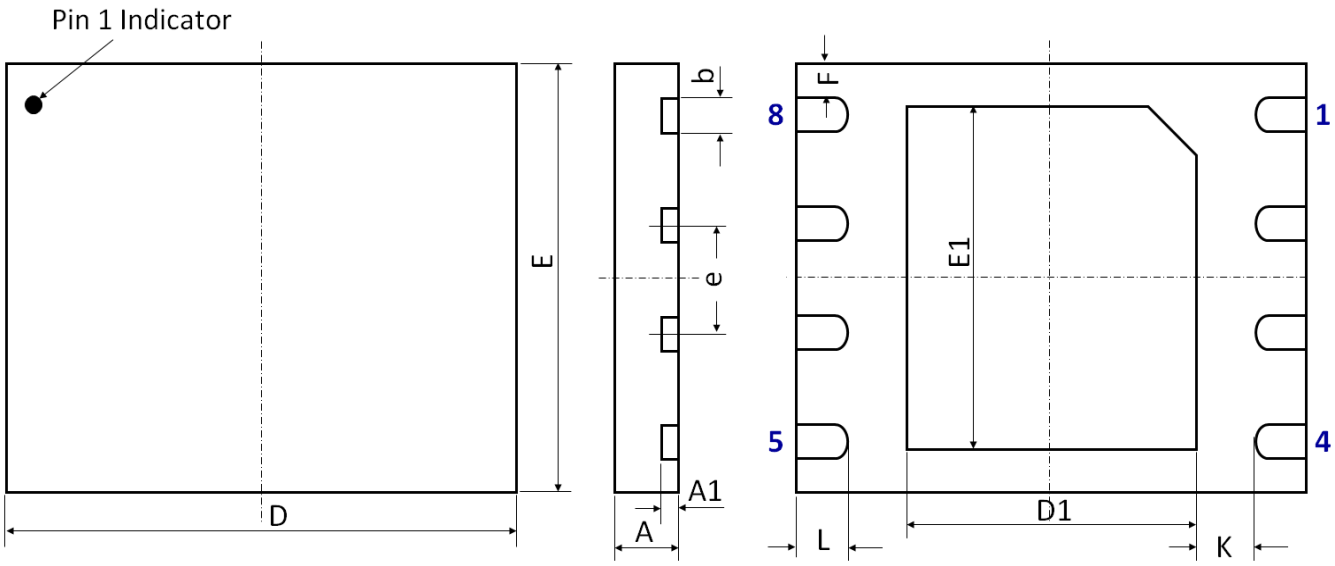


Figure 12.1 Device Package Drawing
(All dimensions are in mm)

Table 12.1 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.75	±0.05	E	5.00 BSC	±0.05
A1	0.203	±0.02	E1	4.00	±0.05
b	0.40	+0.05/-0.07	F	0.395	±0.05
D	6.00 BSC	±0.05	L	0.60	±0.05
D1	3.40	±0.05	K	0.70	±0.05
e	1.27 BSC	±0.05			

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5 µm ~ 20 µm (Typical 10 µm ~ 12 µm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

13.0 PCB Land Design

Guidelines:
[1] 2-layer PCB is recommended.
[2] Via diameter is recommended to be 0.3 mm to prevent solder wicking inside the vias
[3] Thermal vias shall only be placed on the center pad
[4] The maximum via number for the center pad is 7(X)×8(Y)=56

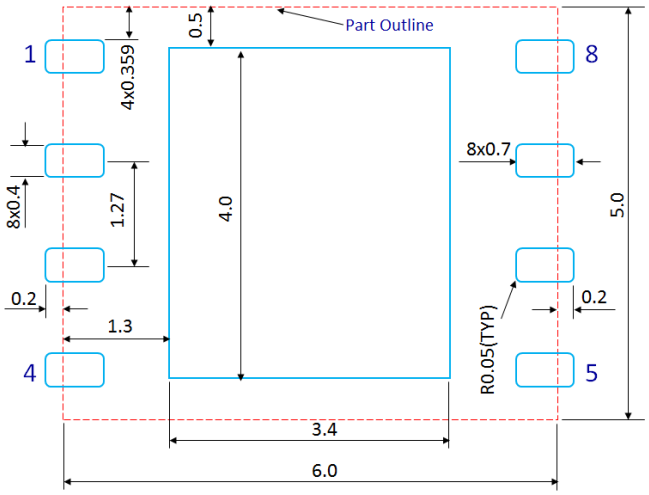


Figure 13.1 PCB Land Pattern
(Dimensions are in mm)

Non-Solder Mask Defined
(Preferred)

Solder Mask Defined

Figure 13.2 Solder Mask Pattern
(Dimensions are in mm)

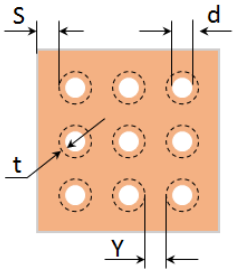


Figure 13.3 Thermal Via Pattern
(Recommended Values: S≥0.15 mm; Y≥0.20 mm; d=0.3 mm; Plating Thickness t=25 µm or 50 µm)

14.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125µm.

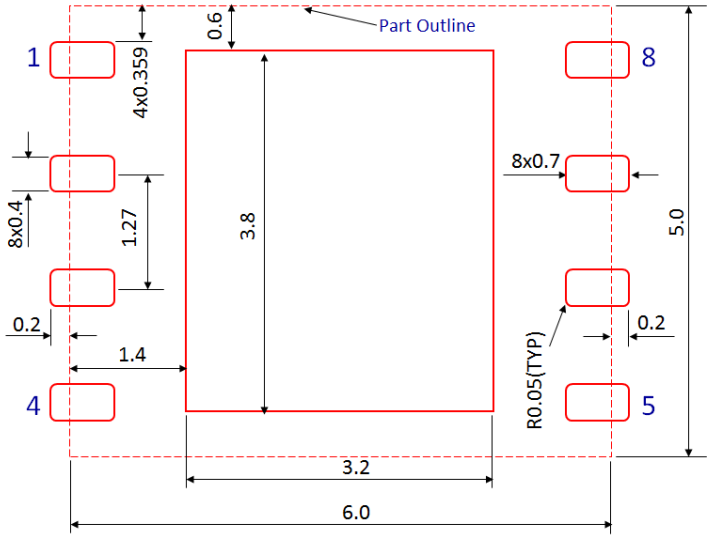


Figure 14.1 Stencil Openings
(Dimensions are in mm)

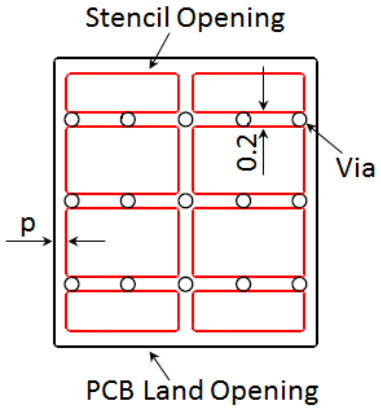


Figure 14.2 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

15.0 Tape and Reel Information

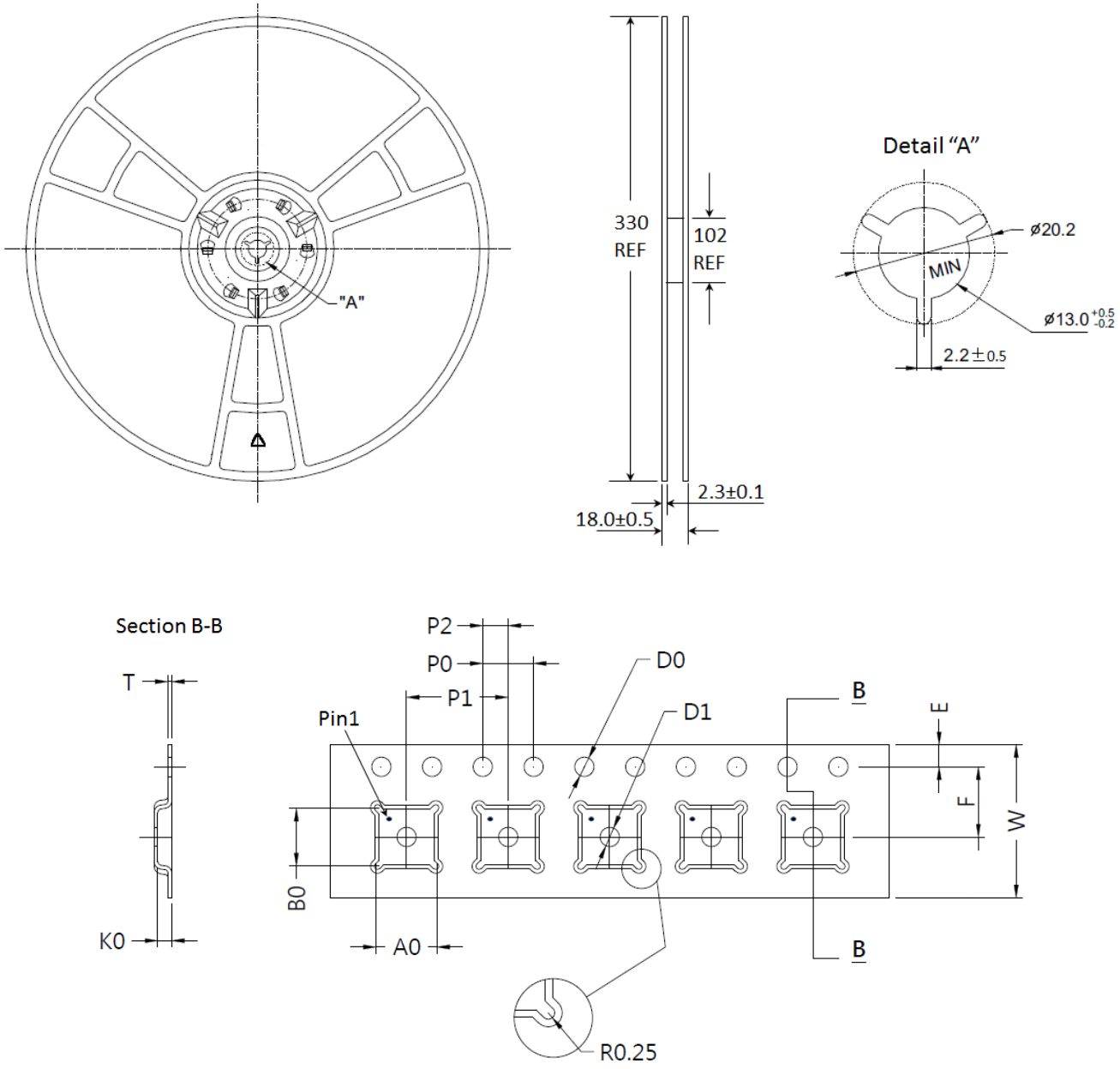


Figure 15.1 Tape and Reel Drawing

Table 15.1 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	6.35	±0.10	K0	1.10	±0.10
B0	5.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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601 W Campus Dr. Ste C1

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