TA9410E – 25 W CW, 50V, 20 – 3000 MHz GaN Power Transistor

1.0 Features

- Small signal gain @ 1000 MHz: 20 dB
- Gain at P3dB @ 1000 MHz: 17 dB
- P3dB @ 1000 MHz: 44 dBm
- PAE @ P3dB @ 1000 MHz: 57%
- 50 V Typical operation
- Operating frequency: 20 MHz to 3.0 GHz

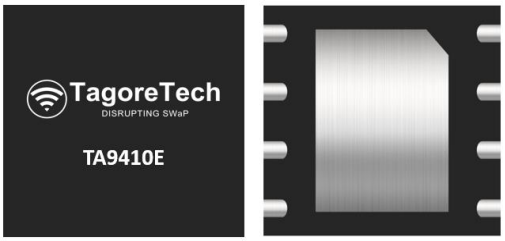


Figure 1.1 Device Image
(8 Pin 6 × 5 × 0.75 mm DFN Package)

2.0 Applications

- Private mobile radio handsets
- Public safety radios
- Cellular infrastructure
- Military radios

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TA9410E is a broadband GaN power transistor capable of delivering 25 W CW from 20 MHz to 3.0 GHz frequency band. The input and output can be matched for best power and efficiency for the desired band.

The TA9410E is packaged in a compact, low-cost Dual Flat No lead (DFN) 5 x 6 x 0.75 mm, 8 leads plastic package.

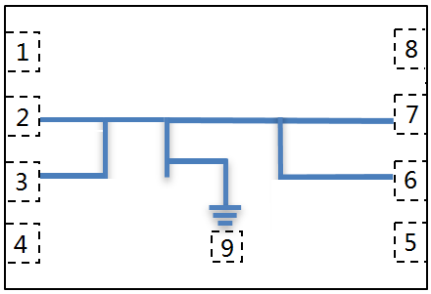


Figure 3.1 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 4.1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TA9410E	8 Pin 5 × 6 × 0.75 mm DFN	Tape and Reel	1000	13” (330 mm)	18 mm	TA9410EMTRPBF
Tuned Evaluation Board, 20 – 525 MHz						TA9410E-EVB-A
Tuned Evaluation Board, 20 – 1000 MHz						TA9410E-EVB-B
Tuned Evaluation Board, 1400 – 2400 MHz						TA9410E-EVB-C
Tuned Evaluation Board, 30 – 800 MHz						TA9410E-EVB-D
Tuned Evaluation Board, 5100 – 5300 MHz						TA9410E-EVB-E
Tuned Evaluation Board, 3400 – 3800 MHz						TA9410E-EVB-F

Tuned Evaluation Board, 30 – 48 MHz	TA9410E+ 2xTS8441L-EVB-G RF1
Tuned Evaluation Board, 48 – 78 MHz	TA9410E+ 2xTS8441L-EVB-G RF2
Tuned Evaluation Board, 78 – 125 MHz	TA9410E+ 2xTS8441L-EVB-G RF3
Tuned Evaluation Board, 125 – 200 MHz	TA9410E+ 2xTS8441L-EVB-G RF4
Tuned Evaluation Board, 200 – 320 MHz	TA9410E+ 2xTS8441L-EVB-G RF5
Tuned Evaluation Board, 320 – 520 MHz	TA9410E+ 2xTS8441L-EVB-G RF6
Tuned Evaluation Board, 330 – 860 MHz	TA9410E-EVB-J
Tuned Evaluation Board, 500 – 2500 MHz	TA9410E-EVB-K

5.0 Pin Description

Table 5.1 Pin Definition

Pin Number	Pin Name	Description
1, 4, 5, 8	NC	No internal connection, can be grounded
2, 3	V_{GG} & RF_{IN}	Gate voltage and RF input
6, 7	V_{DD} & RF_{OUT}	Drain voltage and RF output
9[1]	Paddle/Slug	Ground

Note: [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heat sinking required.

6.0 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Breakdown voltage	V_{DS}	+150	V
Gate voltage	V_{GS}	-10 to +2.0	V
Drain current	I_{DS}	3.0	A
Gate current	I_{GS}	5.2	mA
Power dissipation CW	P_{diss}	28	W
RF input power CW, 20-1000MHz	RF_{IN}	29	dBm
Storage Temperature Range	T_{st}	-55 to +150	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+225	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	5.0	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1A	250 to <500	V
Charged Device Model (CDM)	Level C1	250 to <500	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:
Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 RF Electrical Specifications

Table 7.1 Electrical Specifications @T_A=+25°C Unless Otherwise Specified.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Small Signal Gain	1000 MHz		20		dB
Large Signal Gain	P_{OUT} = 44 dBm, 1000 MHz		17		dB
P3dB	1000 MHz		44		dBm
Power Added Efficiency (PAE)	P_{OUT} = 44 dBm		57		%
Drain Voltage			50		V
Ruggedness	All phase, P_{OUT} = 44 dBm, 1000 MHz	VSWR 10:1			

Note: Data taken from 20 – 1000 MHz broadband reference design (EVB), V_D=+50 V; I_{DQ}=50 mA, CW

8.0 Recommended Operating Conditions

Table 8.1 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltage	V_{DD}		+50		V
Gate Voltage	V_{GG}	-3.3	-2.75	-2.1	V
Drain Bias Current	I_{DQ}		50		mA
Drain Current	$I_{DS,}$ Pout = 44 dBm, 1000 MHz		880		mA
Power Dissipation CW [1]	$P_{diss,}$ Pout = 44 dBm, 1000 MHz		20	25	W
Operating Temperature Range		-40	+25	+85	°C

Note: [1] @TC = +85°C

9.0 Bias and Sequencing

Table 9.1 Bias and Sequencing

Turn ON Device	Turn OFF Device
1. Set V_G to -5 V 2. Set V_D to +50 V 3. Adjust V_G to reach required I_{DQ} current 4. Apply RF power	1. Turn RF power off 2. Turn off V_D 3. Turn off V_G

10.0 Typical Characteristics

10.1 20 – 525 MHz EVB A (Vdd = 50 V, Idq = 50 mA, CW)

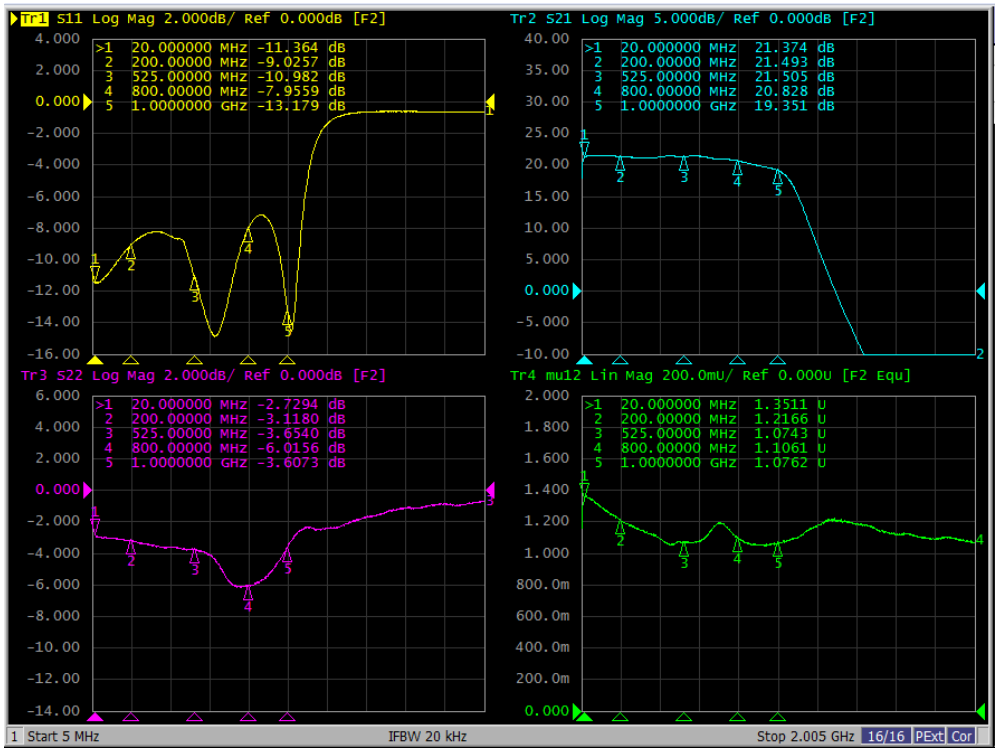


Figure 10.1.1 Small Signal S Parameters (T_A=+25°C)

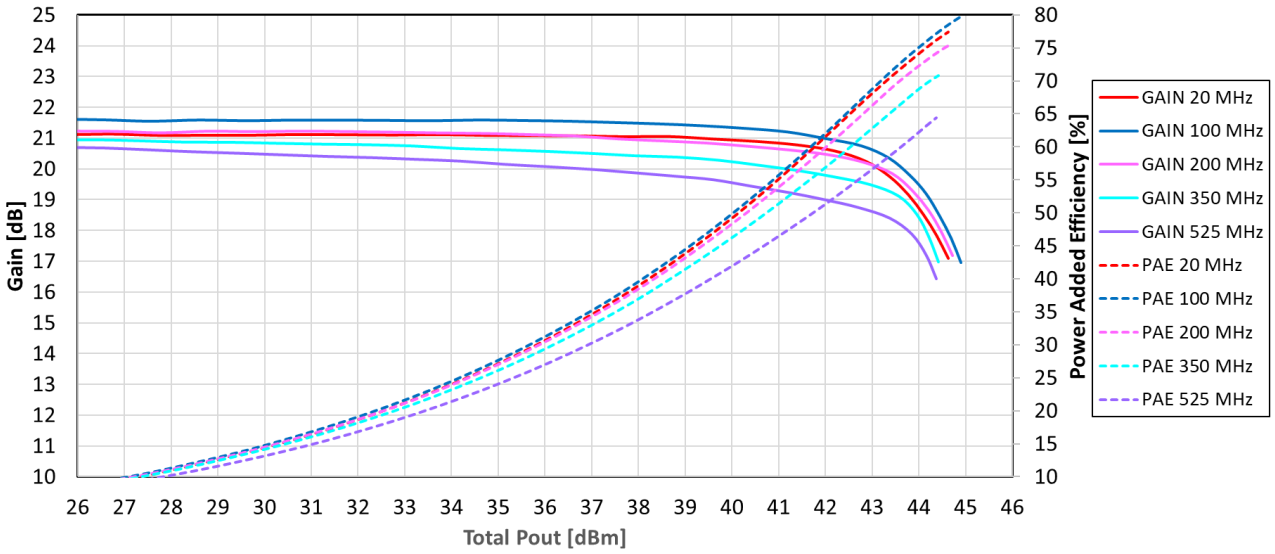


Figure 10.1.2 Gain and PAE vs P_{OUT} (T_A=+25°C)

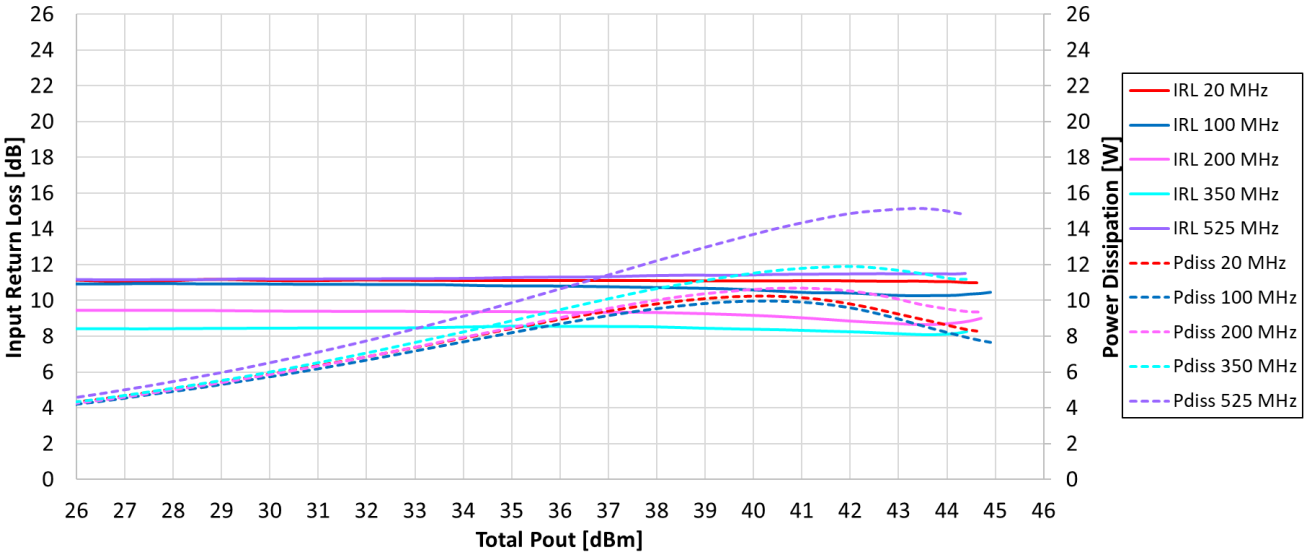


Figure 10.1.3 IRL and Pdiss vs P_{OUT} (T_A=+25°C)

10.2 20 – 1000 MHz EVB B (Vdd = 50 V, Idq = 50 mA, CW)

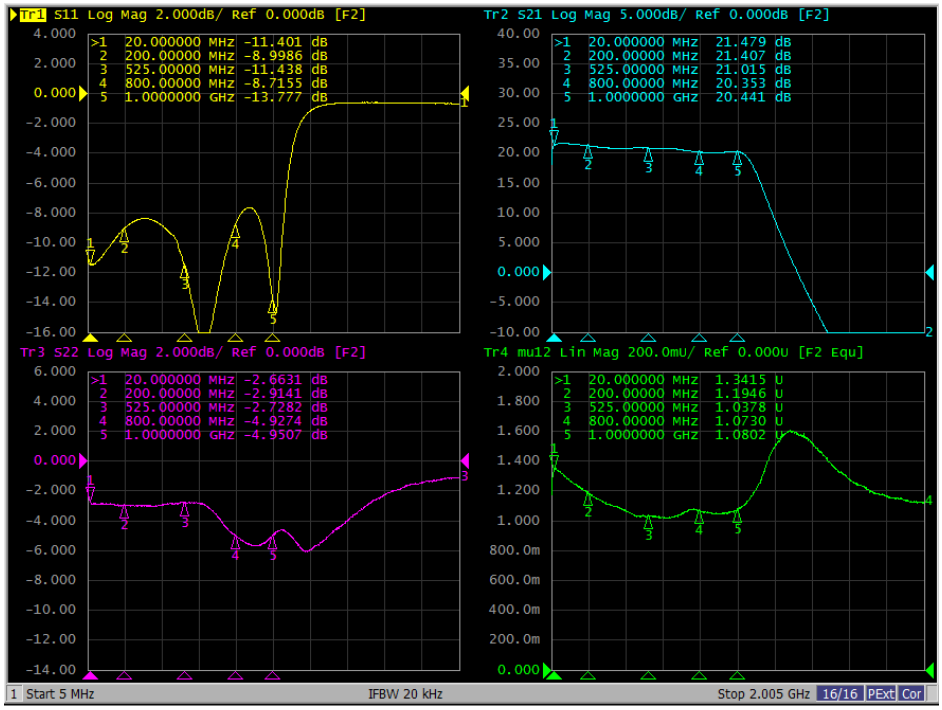


Figure 10.2.1 Small Signal S Parameters (T_A=+25°C)

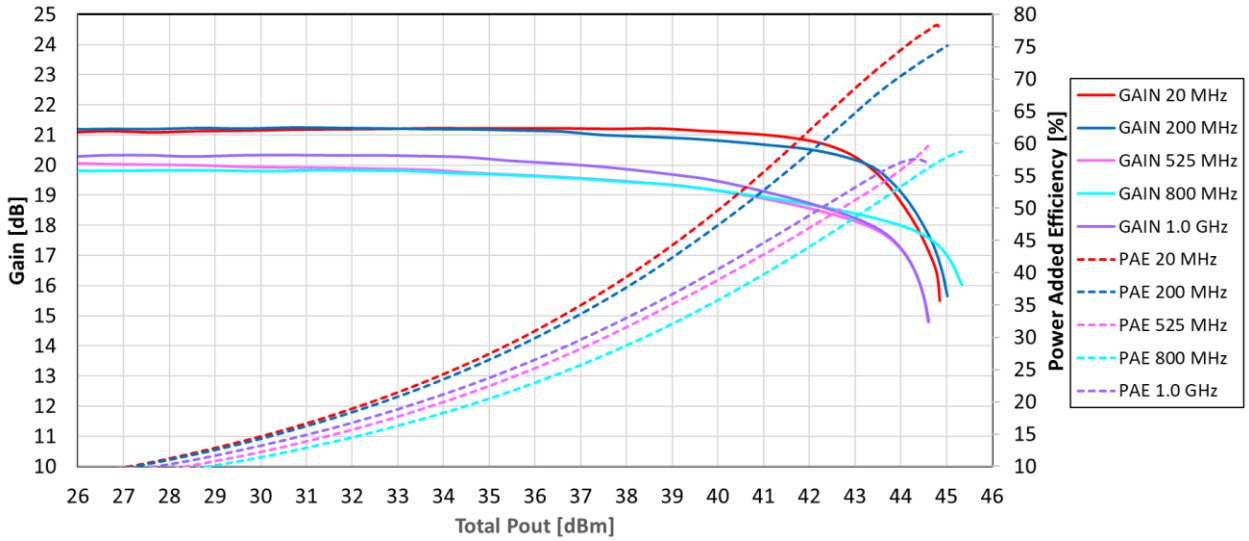


Figure 10.2.2 Gain and PAE vs P_{OUT} (T_A=+25°C)

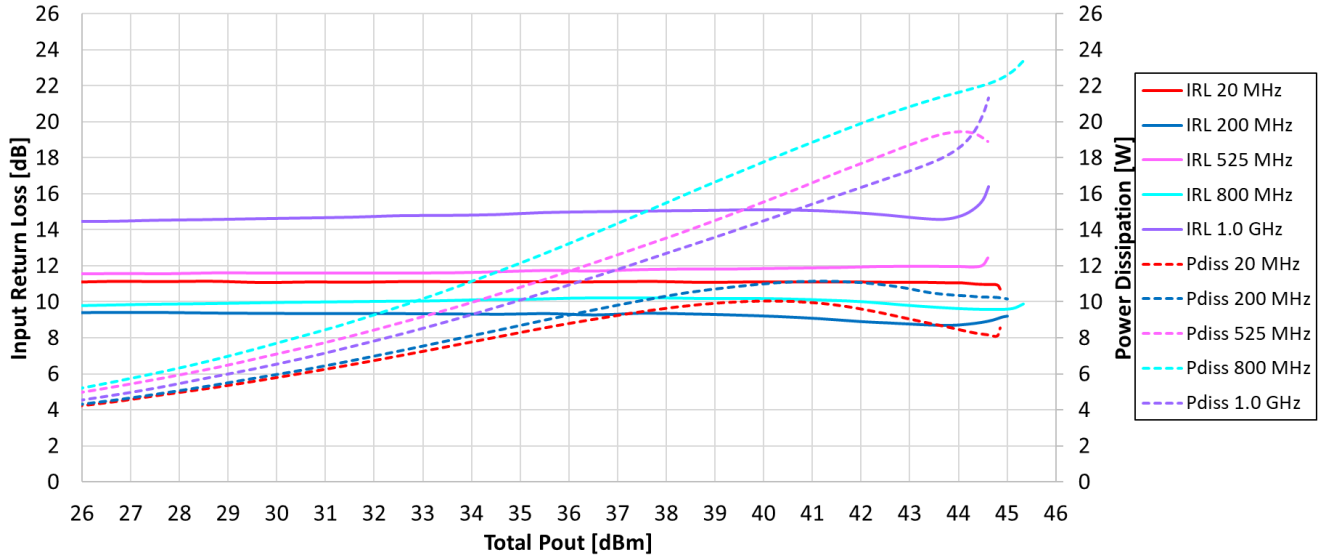


Figure 10.2.3 IRL and Pdiss vs P_{OUT} (T_A=+25°C)

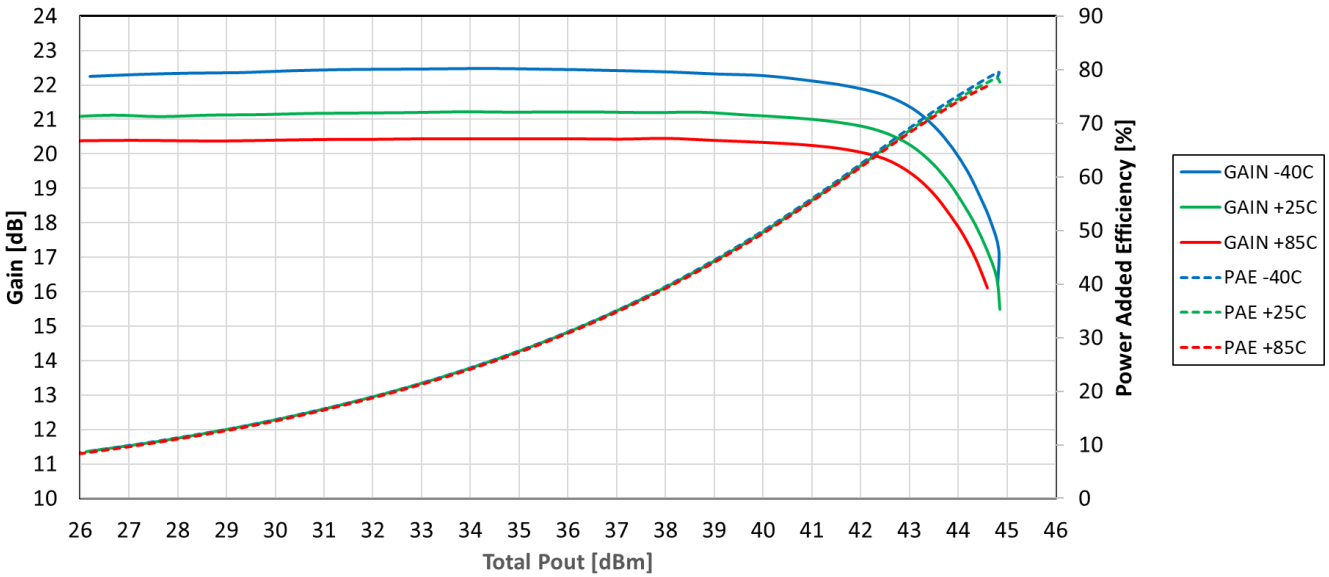


Figure 10.2.4 Gain and PAE vs P_{OUT} over temperature at 20 MHz

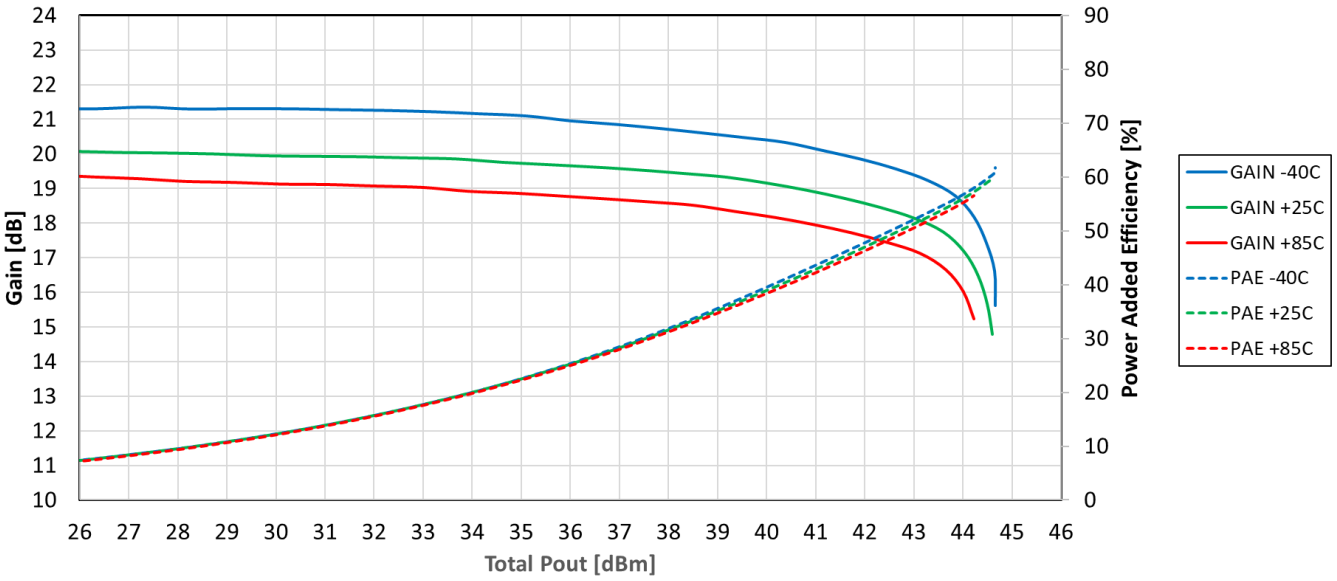


Figure 10.2.5 Gain and PAE vs P_{OUT} over temperature at 525 MHz

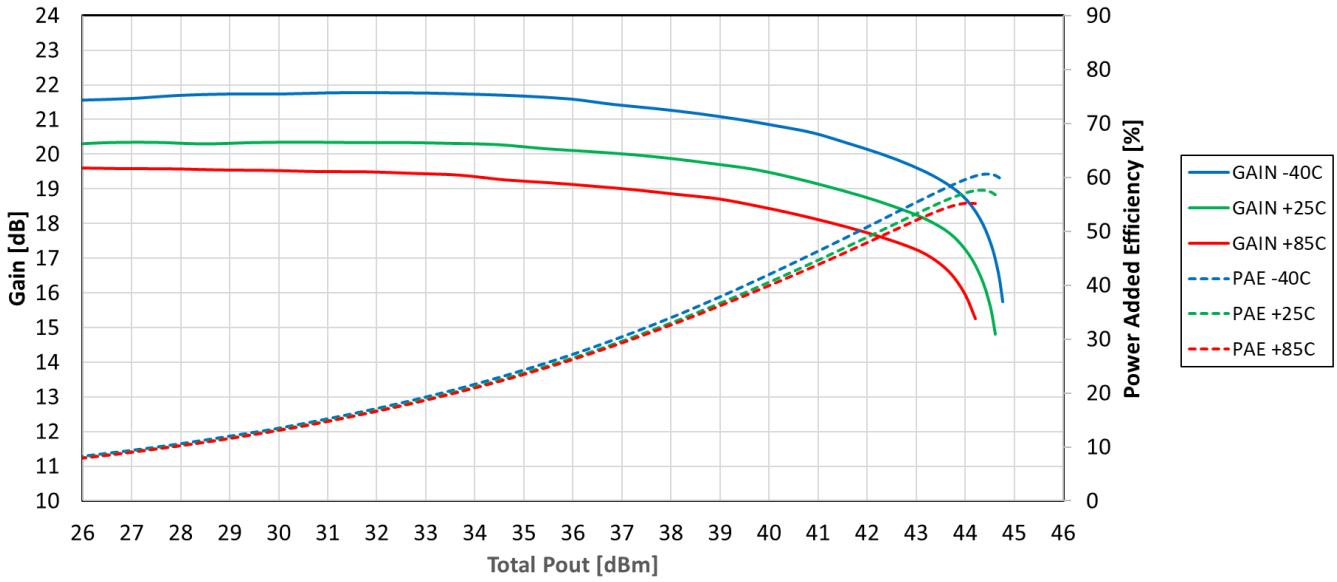


Figure 10.2.6 Gain and PAE vs P_{OUT} over temperature at 1000 MHz

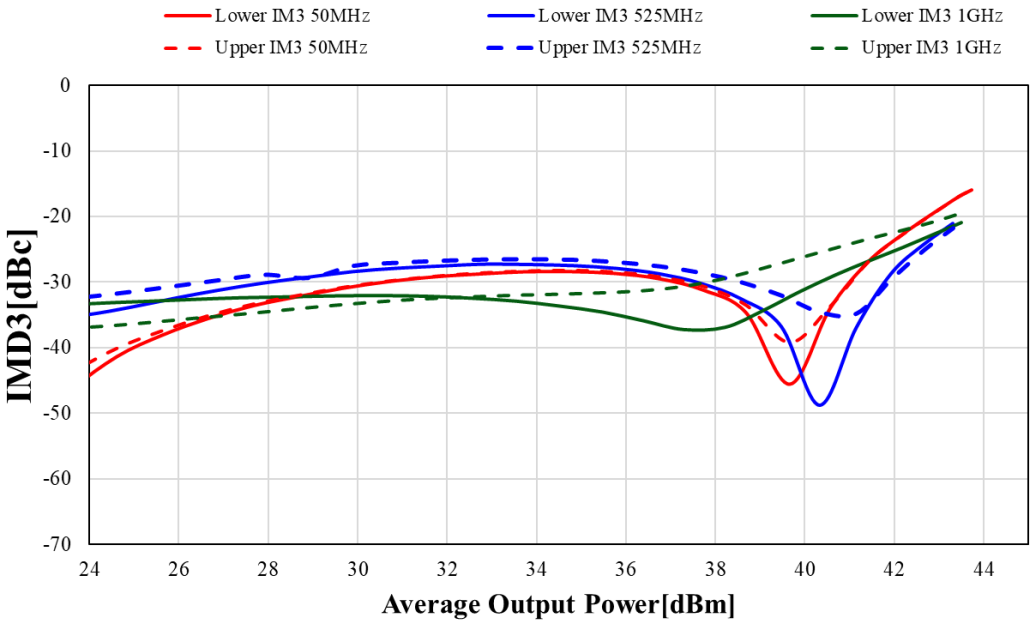


Figure 10.2.7 IMD3 vs P_{OUT} (Vdd=50 V, Idq = 50 mA, 1 MHz tone spacing)

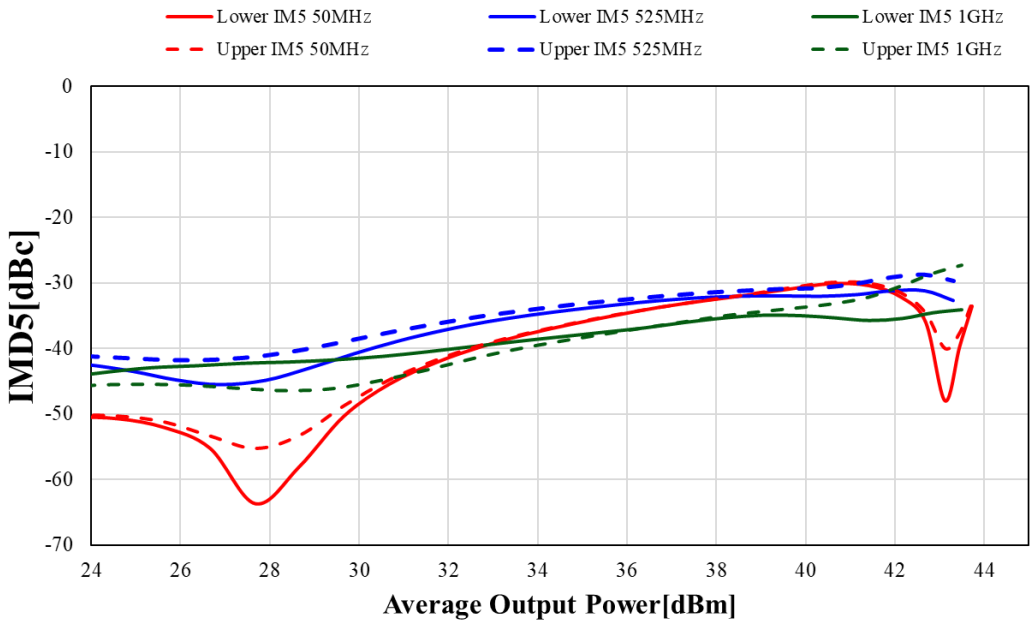


Figure 10.2.8 IMD5 vs P_{OUT} (Vdd=50 V, Idq = 50 mA, 1 MHz tone spacing)

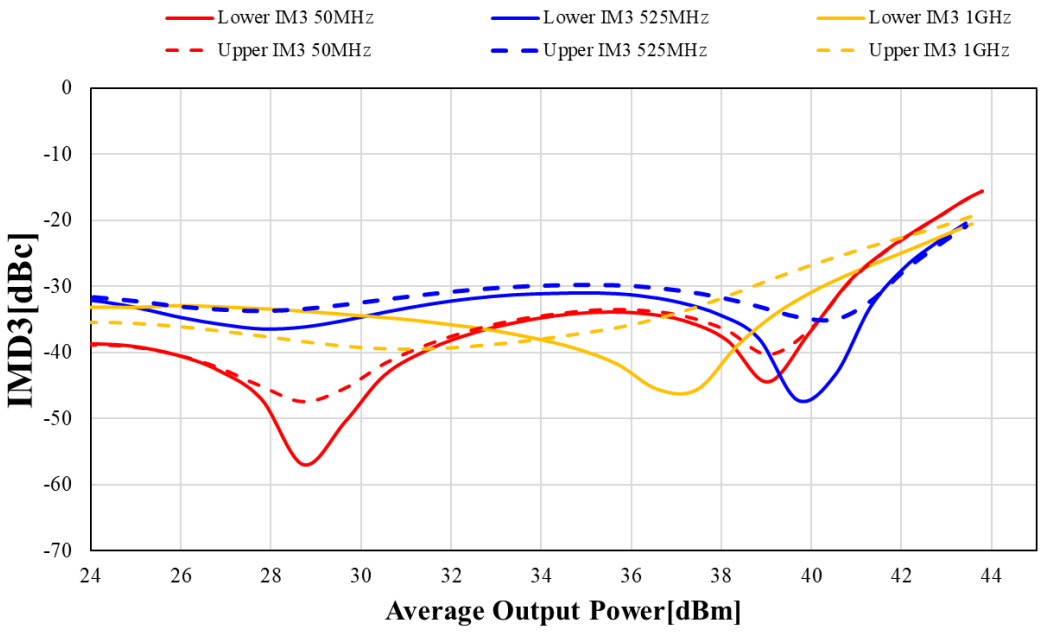


Figure 10.2.9 IMD3 vs P_{OUT} (Vdd=50 V, Idq = 75 mA, 1 MHz tone spacing)

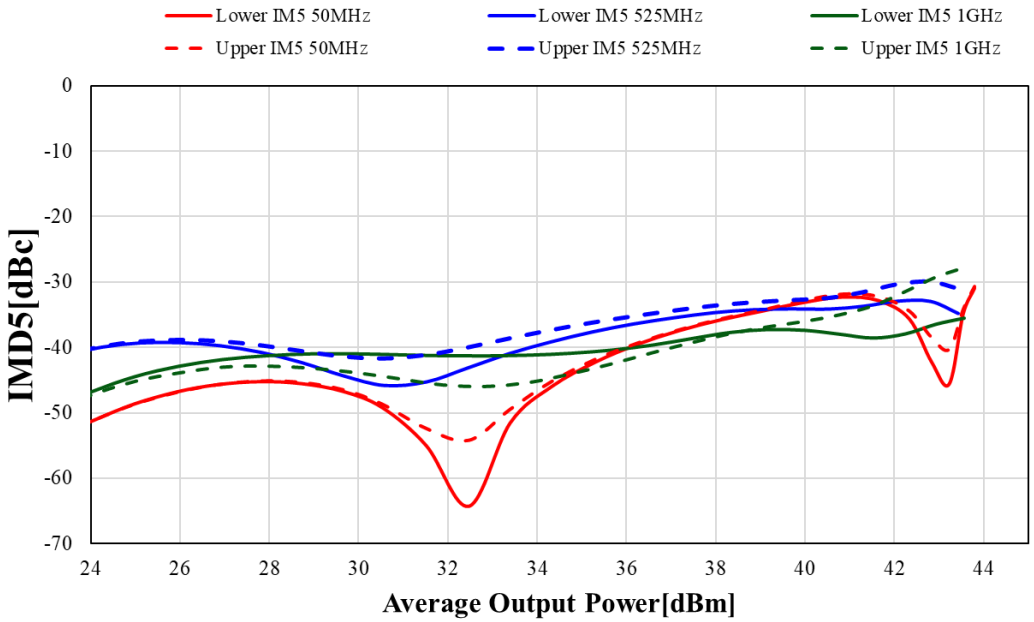


Figure 10.2.10 IMD5 vs P_{OUT} (Vdd=50 V, Idq = 75 mA, 1 MHz tone spacing)

11.0 Evaluation Boards

11.1 20 - 525MHz EVB A

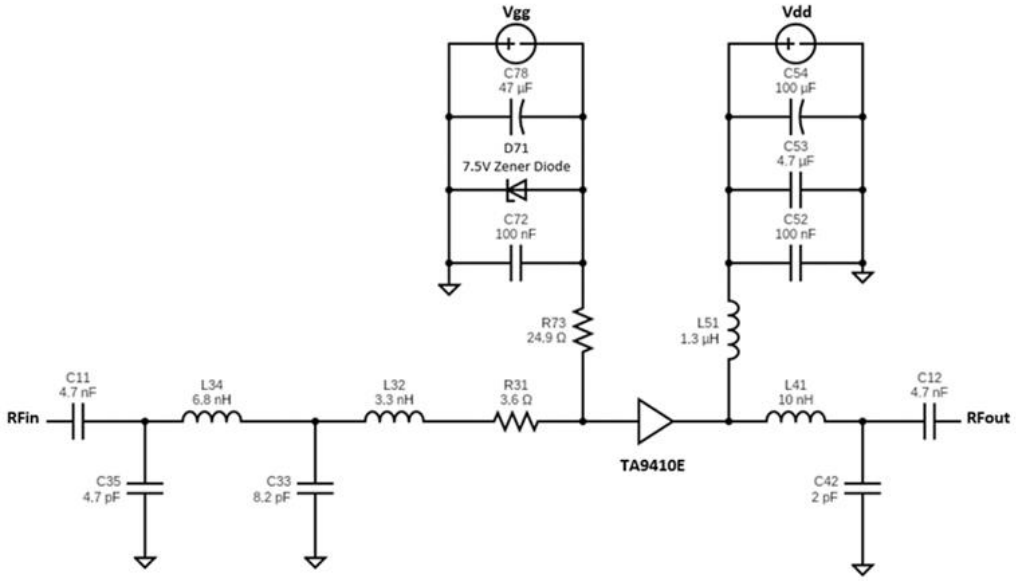
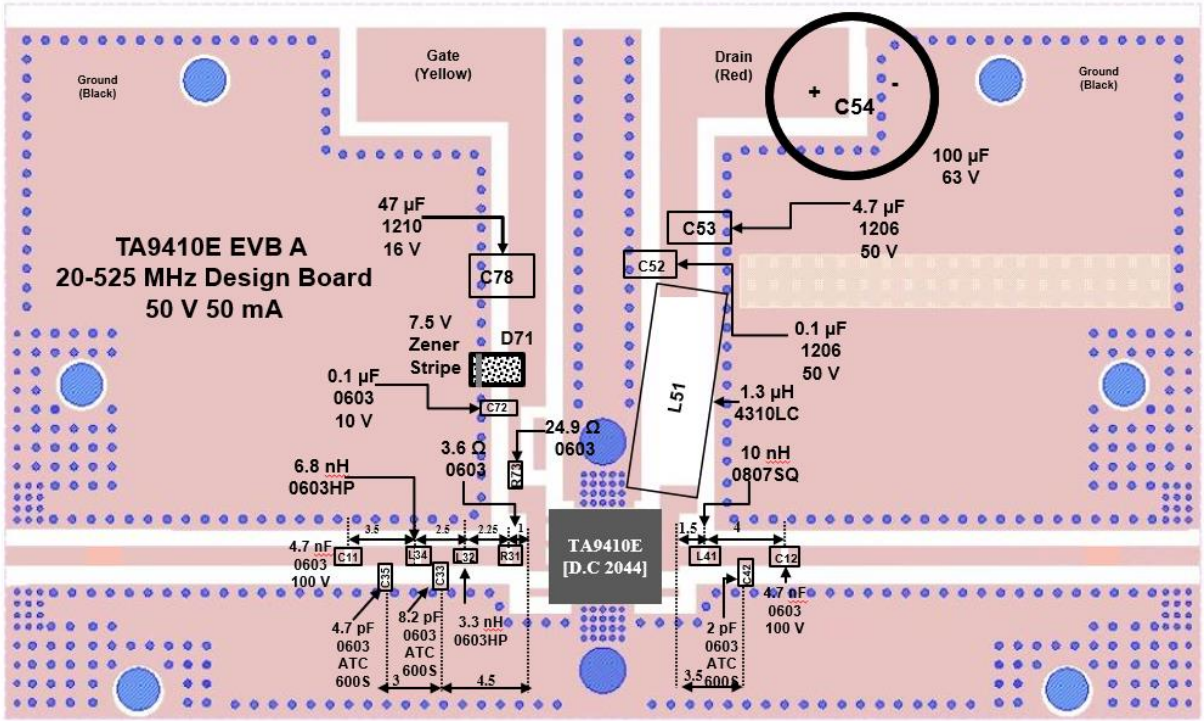


Figure 11.1.1 Schematic of the 20 – 525 MHz EVB A



Note: Pins 4 and 5 can be grounded

Figure 11.1.2 Board Layout of the 20 – 525 MHz EVB A

Table 11.1.1 BOM of the 20 – 525 MHz EVB A

Component ID	Value	Manufacturer	Recommended Part Number
C11, C23	4.7 nF, 100 V	Murata	GCD188R72A472KA01
C12	4.7 pF	ATC	600S4R7BT250XT
L11	6.8 nH	Coil craft	0603HP-6N8XJLC
L12	3.3 nH	Coil craft	0603HP-3N3XJLC
C13	8.2 pF	ATC	600S8R2CT250XT
C14, C21	0.1 µF, 100 V	Murata	GRM31C5C2A104JA01
L21	1.3 µH	Coil craft	4310LC-132KEC
C24	4.7 µF, 100 V	Murata	GCM32DC72A475KE02
L23	10 nH	Coil craft	0807SQ-10NJLC
C22	2.0 pF	ATC	600S2R0BT250XT
R11	3.6 Ω, 0.5 W	Panasonic	ERJ-P06J3R6V
R12	24.9 Ω, 0.75 W	Vishay	CRCW121024R9FKEAHP
D11	7.5 V Zener	On Semiconductor	SZMMSZ5236BT 1G
Q1	25 W GaN Transistor	Tagore Tech	TA9410E
PCB	Rogers RO4350B, 20 mils, 2 oz copper		

11.2 20 – 1000 MHz EVB B

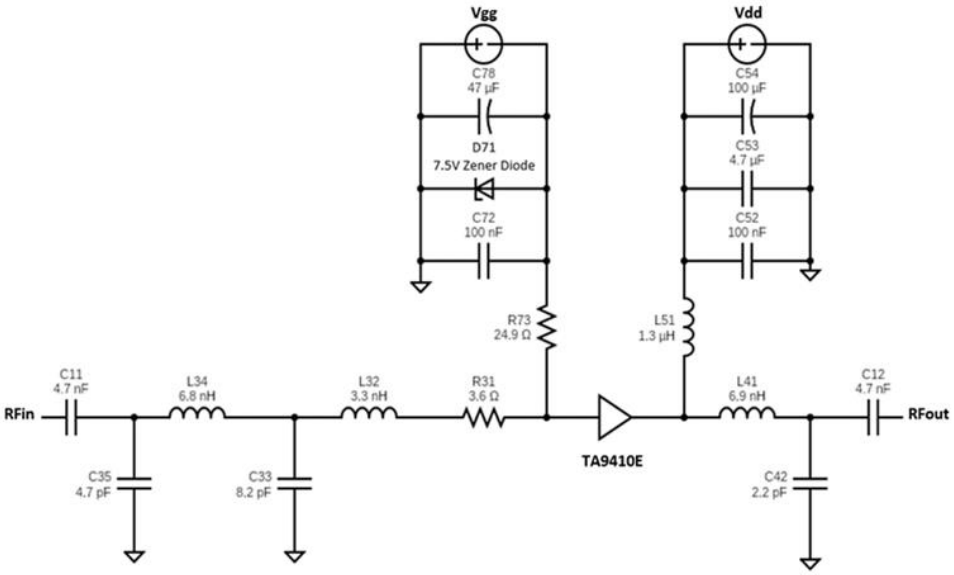
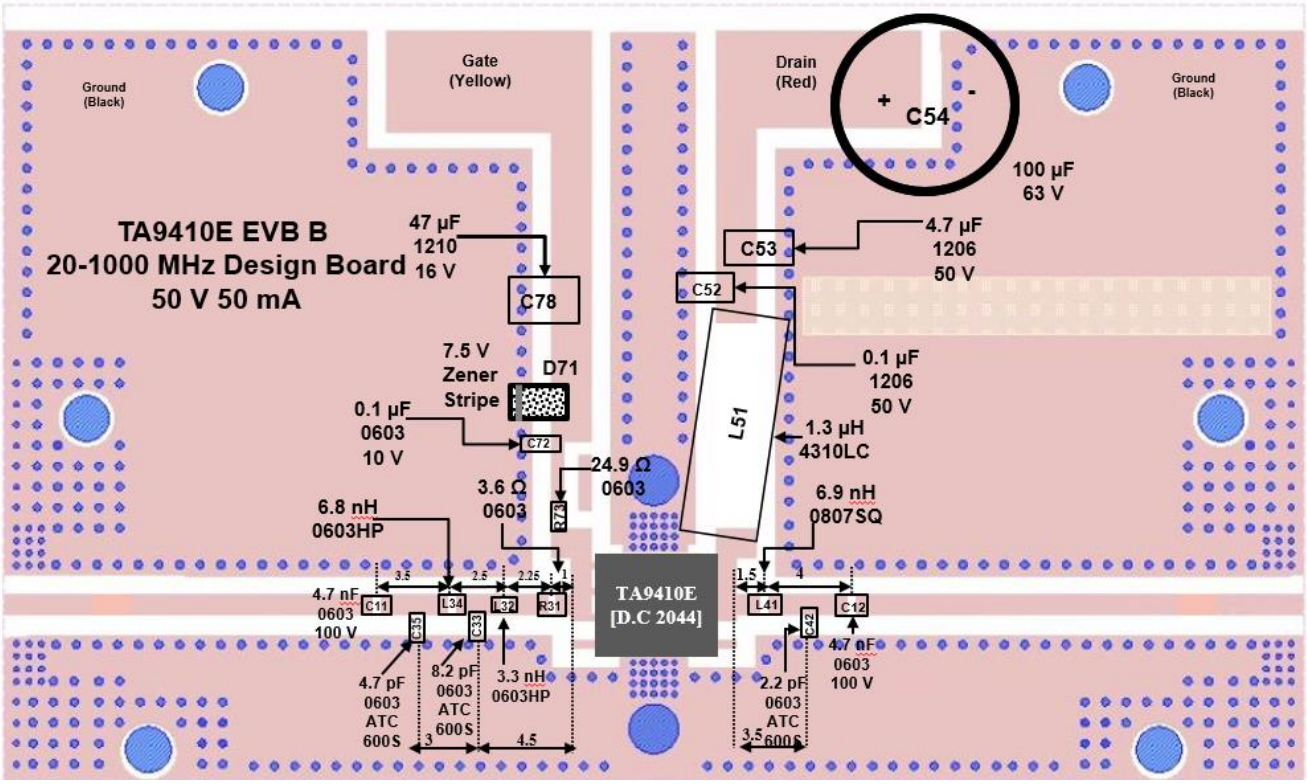


Figure 11.2.1 Schematic of the 20 – 1000 MHz EVB B



Note: Pins 4 and 5 can be grounded

Figure 11.2.2 Board Layout of the 20 – 1000 MHz EVB B

Table 11.2.1 BOM of the 20 – 1000 MHz EVB B

Component ID	Value	Manufacturer	Recommended Part Number
C11, C23	4.7 nF, 100 V	Murata	GCD188R72A472KA01
C12	4.7 pF	ATC	600S4R7BT250XT
L11	6.8 nH	Coil craft	0603HP-6N8XJLC
L12	3.3 nH	Coil craft	0603HP-3N3XJLC
C13	8.2 pF	ATC	600S8R2CT250XT
C14, C21	0.1 µF, 100 V	Murata	GRM31C5C2A104JA01
L21	1.3 µH	Coil craft	4310LC-132KEC
C24	4.7 µF, 100 V	Murata	GCM32DC72A475KE02
L23	6.9 nH	Coil craft	0807SQ-6N9JLC
C22	2.2 pF	ATC	600S2R2BT250XT
R11	3.6 Ω, 0.5 W	Panasonic	ERJ-P06J3R6V
R12	24.9 Ω, 0.75 W	Vishay	CRCW121024R9FKEAHP
D11	7.5 V Zener	On Semiconductor	SZMMSZ5236BT 1G
Q1	25 W GaN Transistor	Tagore Tech	TA9410E
PCB	Rogers RO4350B, 20 mils, 2 oz copper		

12.0 Device Package Information

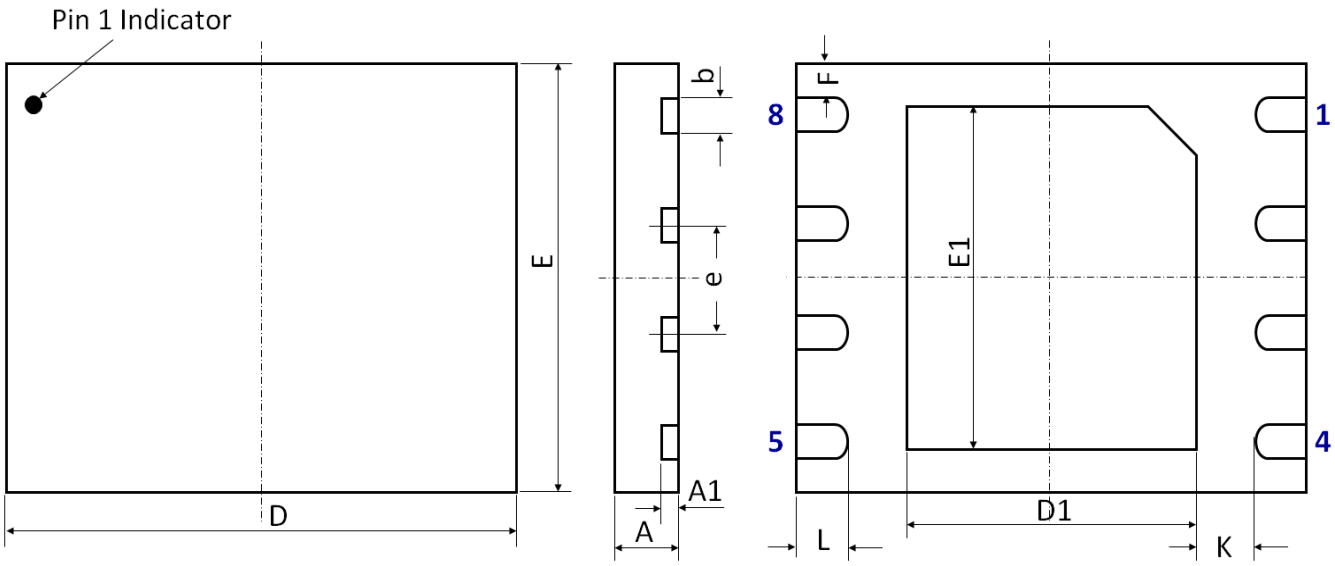


Figure 12.1 Device Package Drawing
(All dimensions are in mm)

Table 12.1 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.75	±0.05	E	5.00 BSC	±0.05
A1	0.203	±0.02	E1	4.00	±0.05
b	0.40	+0.05/-0.07	F	0.395	±0.05
D	6.00 BSC	±0.05	L	0.60	±0.05
D1	3.40	±0.05	K	0.70	±0.05
e	1.27 BSC	±0.05			

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5 µm ~ 20 µm (Typical 10 µm ~ 12 µm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

13.0 PCB Land Design

Guidelines:
[1] 2-layer PCB is recommended.
[2] Via diameter is recommended to be 0.3mm to prevent solder wicking inside the vias
[3] Thermal vias shall only be placed on the center pad
[4] The maximum via number for the center pad is 7(X)×8(Y)=56

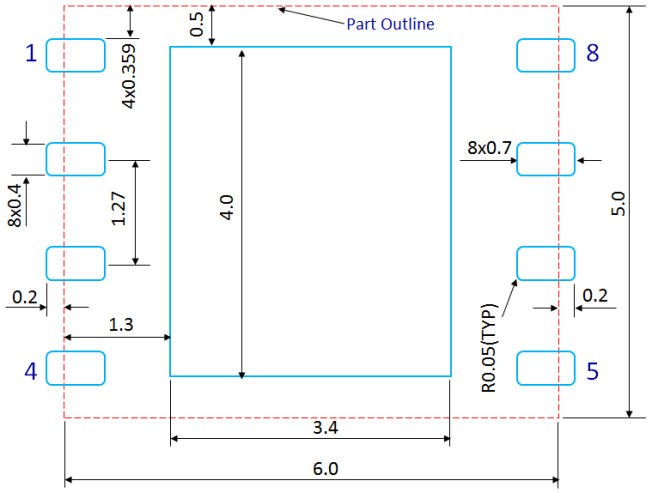


Figure 13.1 PCB Land Pattern
(Dimensions are in mm)

Non-Solder Mask Defined
(Preferred)

Solder Mask Defined

Figure 13.2 Solder Mask Pattern
(Dimensions are in mm)

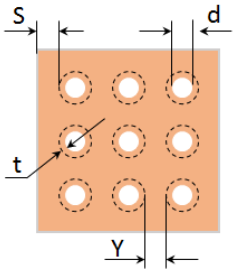


Figure 13.3 Thermal Via Pattern
(Recommended Values: S≥0.15 mm; Y≥0.20 mm; d=0.3 mm; Plating Thickness t=25 µm or 50 µm)

14.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125 µm.

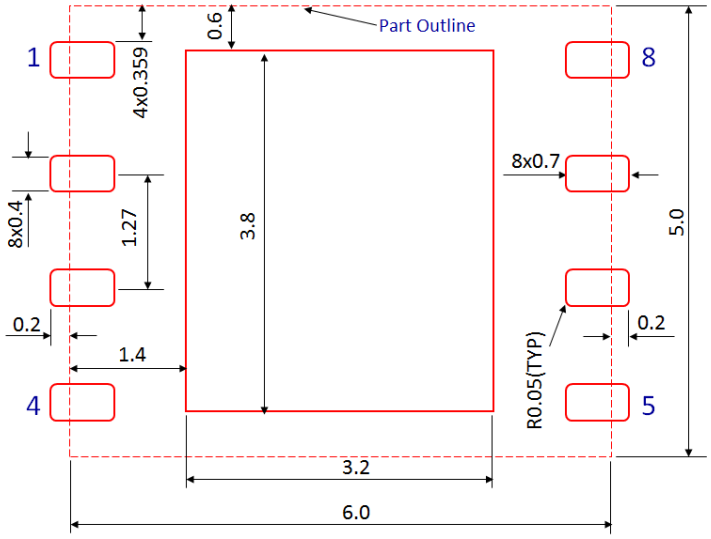


Figure 14.1 Stencil Openings
(Dimensions are in mm)

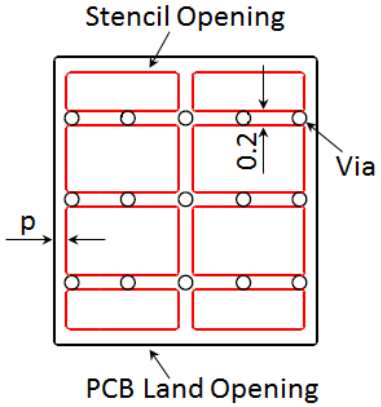


Figure 14.2 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

15.0 Tape and Reel Information

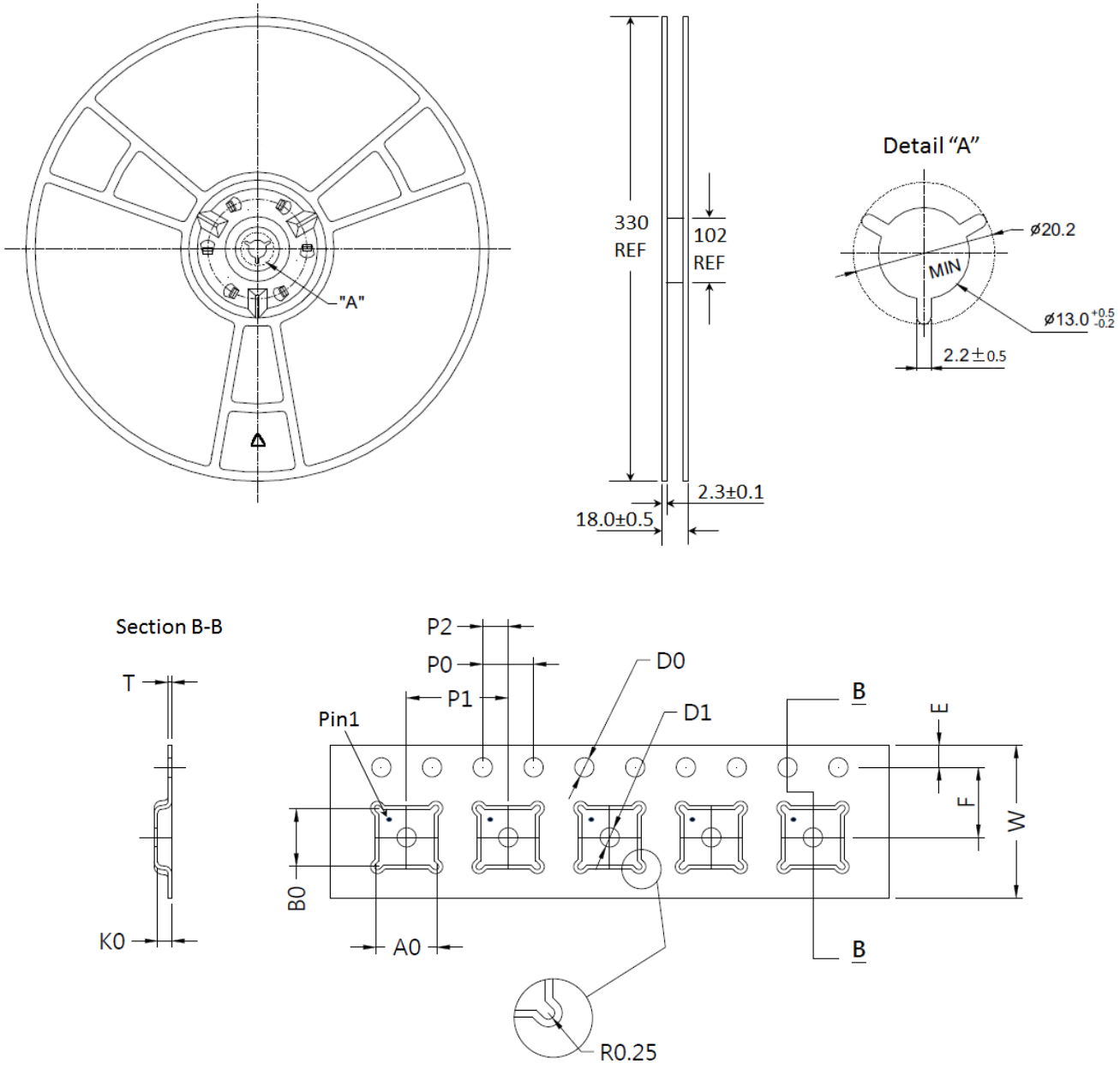


Figure 15.1 Tape and Reel Drawing

Table 15.1 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	6.35	±0.10	K0	1.10	±0.10
B0	5.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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