TP0310K – 27 dBm (0.5 W) CW, 0.03 – 3.8 GHz Power Low Noise Amplifier

1.0 Features

- Small signal gain @ 1850 MHz: 16.5 dB
- NF @ 1850 MHz: 1.0 dB
- OP1dB @ 1850 MHz: 27.5 dBm
- OIP3dB @ 1850 MHz: 39 dBm
- 5 V Typical operating voltage
- Operating frequency: 0.03 to 3.8 GHz

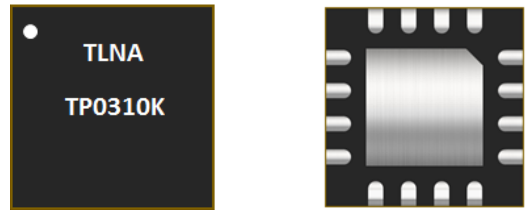


Figure 1.1 Device Image
(16 Pin 3 × 3 × 0.8 mm QFN Package)

2.0 Applications

- 4G/5G Infrastructure Radios
- Small Cells and Cellular Repeaters
- L, S band Phase Array Radar
- Mil/Comms Radios
- SDARS

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TP0310K is a power Low Noise Amplifier (LNA) providing high gain and linearity. With a simple input and output match, this LNA can be tuned for different frequency bands targeting low noise, high power, and high linearity over 0.03-3.8 GHz frequency band.

At 1.85 GHz, the amplifier typically provides 16.5 dB gain, 27.5 dBm OP1, +39 dBm OIP3, and a 1.0 dB noise figure, while drawing 140-160 mA current from a +5 V supply.

The TP0310K is packaged in a compact, low-cost Dual Flat No Lead (QFN) 3 x 3 x 0.8 mm, 16 pin plastic package.

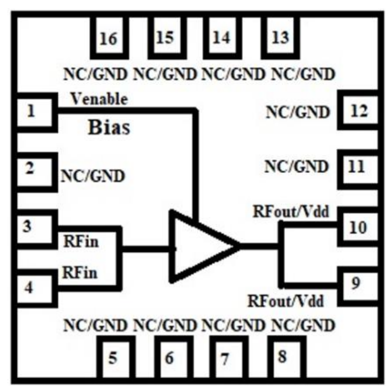


Figure 3.1 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 4.1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TP0310K	16 Pin 3 × 3 × 0.8 mm QFN	Tape & Reel	5000	13" (330 mm)	18 mm	TP0310KMTRPBF
Tuned Evaluation Board, 1700 – 2000 MHz						TP0310K-EVB-A
Tuned Evaluation Board, 2500 – 2700 MHz						TP0310K-EVB-B
Tuned Evaluation Board, 3300 – 3800 MHz						TP0310K-EVB-C
Tuned Evaluation Board, 130 – 950 MHz						TP0310K-EVB-D
Tuned Evaluation Board, 30 – 525 MHz						TP0310K-EVB-E
Tuned Evaluation Board, 2900 – 3500 MHz						TP0310K-EVB-F

5.0 Pin Description

Table 5.1 Pin Definition

Pin Number	Pin Name	Description
2,5-8, 11-16	NC	No internal connection, can be connected to ground
1	Venable	Venable along with series resistor, sets the Idq. Venable <0.2V disables the device
3,4	RF_{IN}	RF Input. DC blocking cap required
9,10	RF_{OUT}/V_{dd}	RF Output. Vdd supplied through an external choke inductor
Package Base	Paddle/Slug	DC and RF Ground. Also provides thermal relief. Multiple vias are recommended

Note: [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heat sinking required.

6.0 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Supply voltage, Venable	V_{dd}	+6	V
Drain current	I_{DQ}	150	mA
RF input power CW	RF_{IN}	23	dBm
Storage Temperature Range	T_{st}	-55 to +150	°C
Operating Temperature Range	T_{op}	-40 to +105	°C
Maximum Junction Temperature	T_J	170	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	10	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:
Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Recommended DC Operating Conditions

Table 7.1 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltage	V_{DD}		+5.0		V
Venable Voltage	V_{enable}		+5.0		V
Drain Bias Current	$I_{DQ,}$ Set by external resistor		140		mA
Venable Bias Current	I_{bias}		3.5	4	mA
Operating Temperature Range		-40	+25	+105	°C

8.0 Switching Time

Table 8.1 Switching time.

Parameter	Test Condition	Typical	Unit
Switching Rise Time	10/90% of the RF value	4	nsec
Switching Fall Time	10/90% of the RF value	1000	nsec

9.0 RF Electrical Specifications

Table 9.1 1700 – 2000 MHz EVB-A @T_A=+25°C Unless Otherwise Specified; Venable = High

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across Band		16-17		dB
Noise Figure	Across Band		1.0		dB
EVB Noise Figure	Across Band		1.05		dB
Input Return Loss	Across Band		11-14		dB
Output Return Loss	Across Band		10-13		dB
OP1dB	Across Band		27-27.5		dBm
OIP3	Across Band, 8 dBm per tone, Tone Spacing 2 MHz		39		dBm

Table 9.2 2500 – 2700 MHz EVB-B @T_A=+25°C Unless Otherwise Specified; Venable = High

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	2600MHz	13	14		dB
Noise Figure	2600MHz		1.1		dB
EVB Noise Figure	2600MHz		1.2		dB
Input Return Loss	2600MHz		16		dB
Output Return Loss	2600MHz		18		dB
OP1dB	2600MHz	25.5	27		dBm
OIP3	@ 2600 MHz, 8 dBm per tone, Tone Spacing 2 MHz	35	37		dBm

Table 9.3 3300 – 3800 MHz EVB-C @T_A=+25°C Unless Otherwise Specified; Venable = High

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across Band		11-11.5		dB
Noise Figure	Across Band		0.85-1.15		dB
EVB Noise Figure	Across Band		1-1.3		dB
Input Return Loss	Across Band		7-11		dB
Output Return Loss	Across Band		17-24		dB
OP1dB	Across Band		27.5		dBm
OIP3	Across Band, 8 dBm per tone, Tone Spacing 2 MHz		41-42		dBm

Table 9.4 130 – 950 MHz EVB-D @T_A=+25°C Unless Otherwise Specified; Venable = High

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across Band		27.6-21		dB
Noise Figure	Across Band		1.5-2.4		dB
EVB Noise Figure	Across Band		1.6-2.5		dB
Input Return Loss	Across Band		6-25		dB
Output Return Loss	Across Band		7-17		dB
OP1dB	Across Band		24.7-27		dBm
OIP3	Across Band, 8 dBm per tone, Tone Spacing 2 MHz		34-37		dBm

Table 9.5 30 – 525 MHz EVB-E @T_A=+25°C Unless Otherwise Specified; Venable = High

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across Band		24-21		dB
Noise Figure	Across Band		2.3-1.7		dB
EVB Noise Figure	Across Band		2.3-1.7		dB
Input Return Loss	Across Band		7-8		dB
Output Return Loss	Across Band		4-6		dB
OP1dB	Across Band		25-26.5		dBm
OIP3	Across Band, 16 dBm per tone, Tone Spacing 2 MHz		37-40		dBm

10.0 Typical Characteristics

10.1 2500 – 2700 MHz tuned EVB-B (Vdd=5 V, I_{DQ}=140 mA), -40ºC, 25ºC, 85ºC, 105 ºC, Narrowband

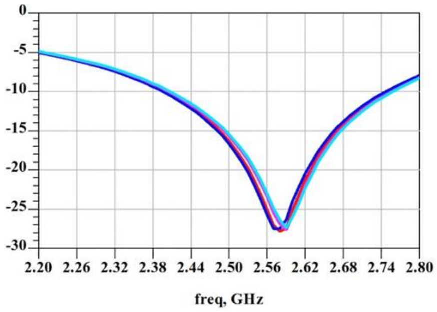


Figure 10.1 S11 vs Freq

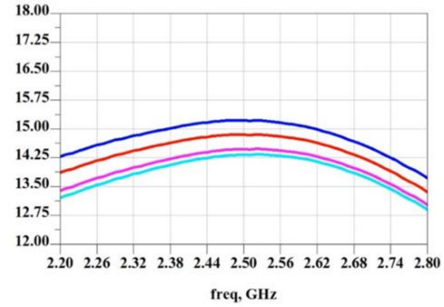


Figure 10.2 S21 vs Freq

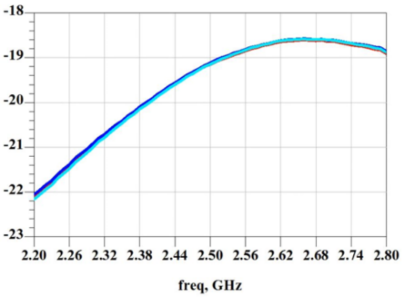


Figure 10.3 S12 vs Freq

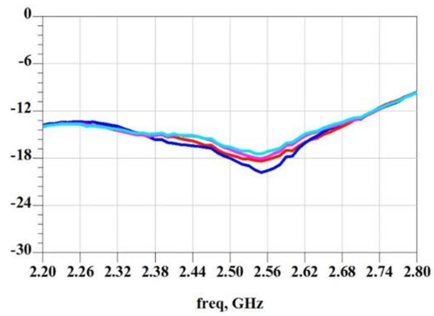


Figure 10.4 S22 vs Freq

-40ºC, 25ºC, 85ºC, 105 ºC, Broadband

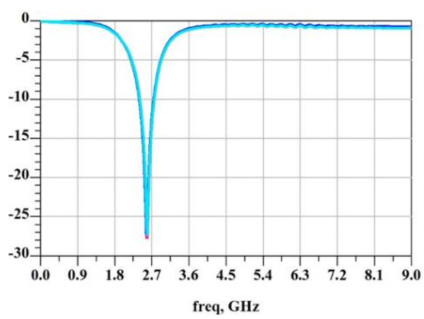


Figure 10.5 S11 vs Freq

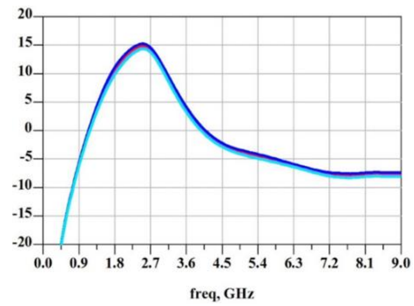


Figure 10.6 S21 vs Freq

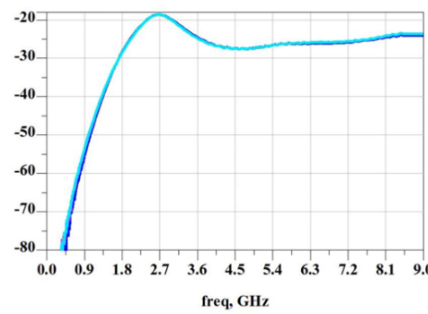


Figure 10.7 S12 vs Freq

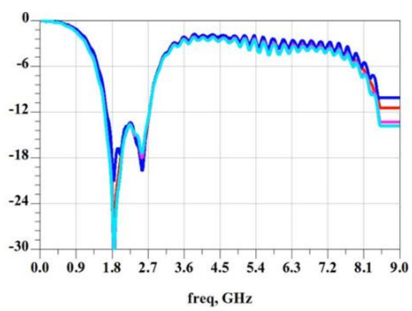


Figure 10.8 S22 vs Freq

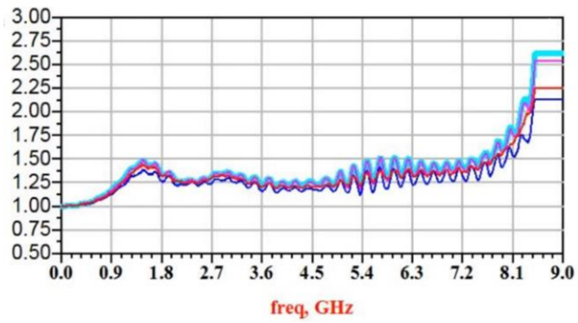


Figure 10.9 Mu1 vs Freq

-40ºC, 25ºC, 85ºC, 105 ºC

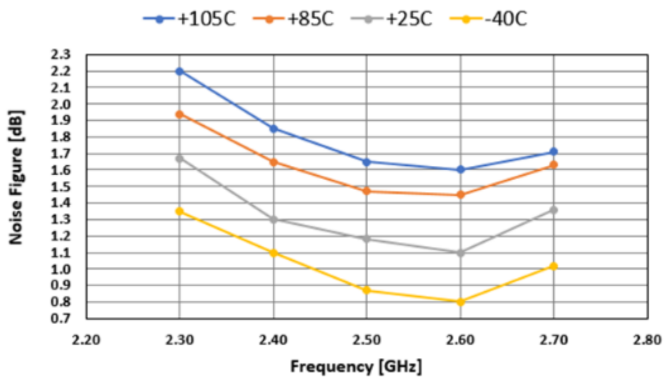


Figure 10.10 Noise Figure (EVB) vs Freq

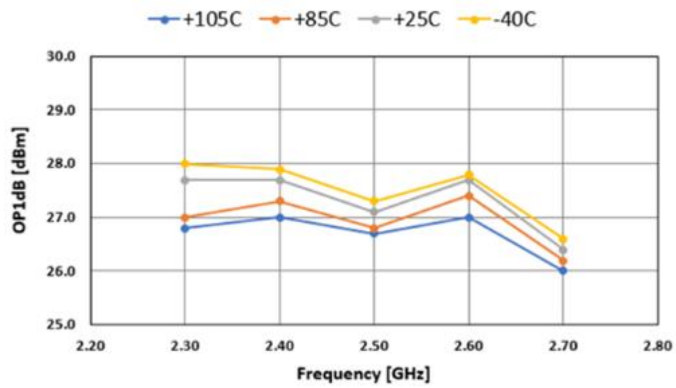


Figure 10.11 Output P1dB vs Freq

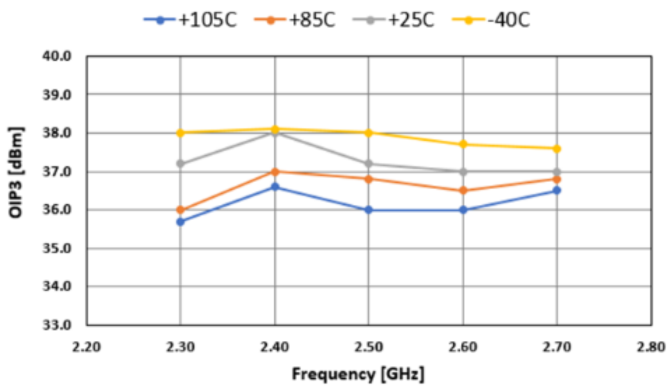


Figure 10.12 Output IP3 vs Freq

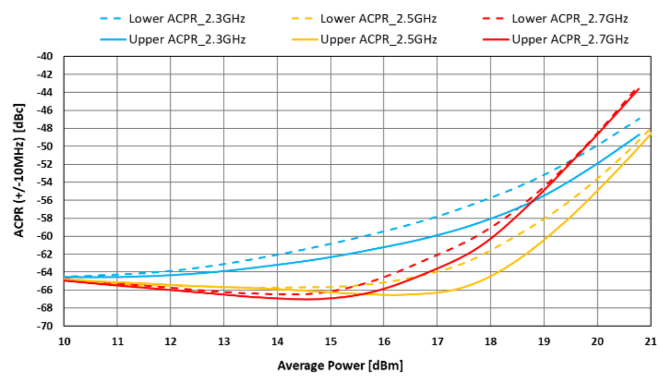


Figure 10.13 ACPR vs Average Power
[8.8dB PAPR 10MHz BW]

11.0 Evaluation Boards

11.1 1700 – 2000 MHz EVB A

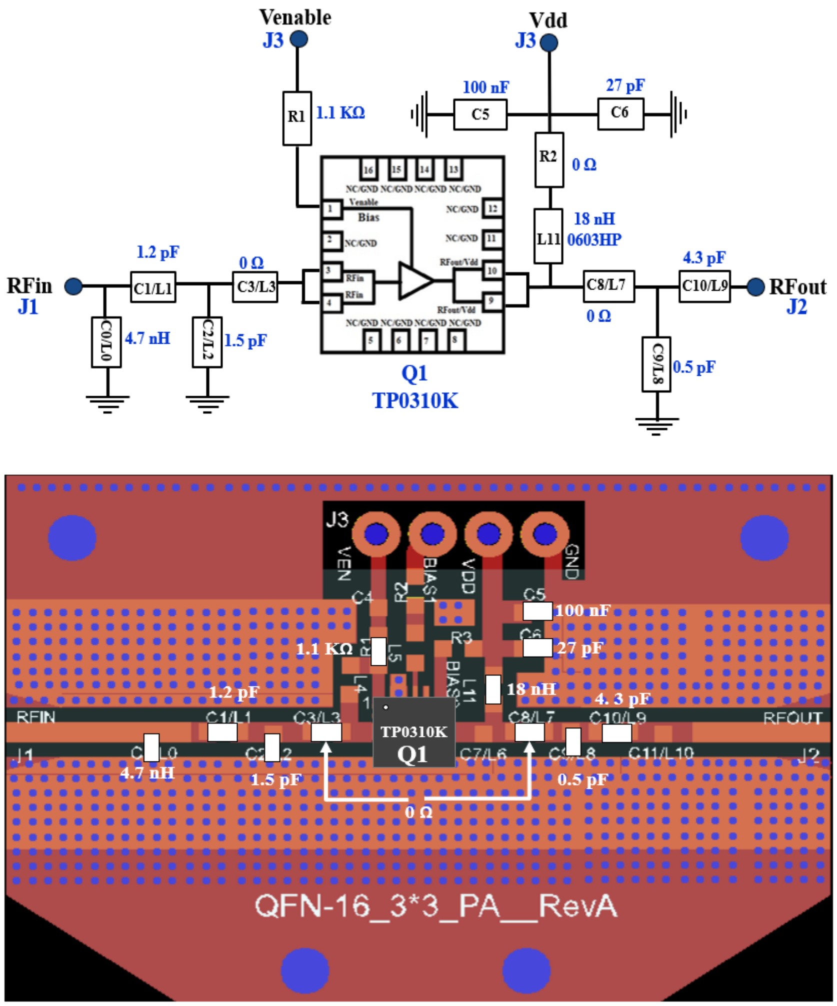


Figure 11.1 Schematic & Layout of the 1700 – 2000 MHz EVB A

Table 11.1 BOM of the 1700 – 2000 MHz EVB A

Component ID	Value	Manufacturer	Recommended Part Number
C0/L0	4.7 nH	Coil craft	0402HP-4N7XGRW
C1/L1	1.2 pF	Murata	GJM1555C1H1R2BB01
C2/L2	1.5 pF	Murata	GJM1555C1H1R5BB01
R1	1.1 KΩ	Panasonic	ERJ-2RKF1101X
C9/L8	0.5 pF	Murata	GJM1555C1HR50BB01
C10/L9	4.3 pF	Murata	GJM1555C1H4R3BB01
L11	18 nH	Coil craft	0402HP-18NXGRW
C5	100 nF	TDK	C1005X7R1H104K050BE
C6	27 pF	Murata	GJM1555C1H270JB01D
Q1	GaAs LNA	Tagore Tech	TP0310K
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

11.2 2500 – 2700 MHz EVB B

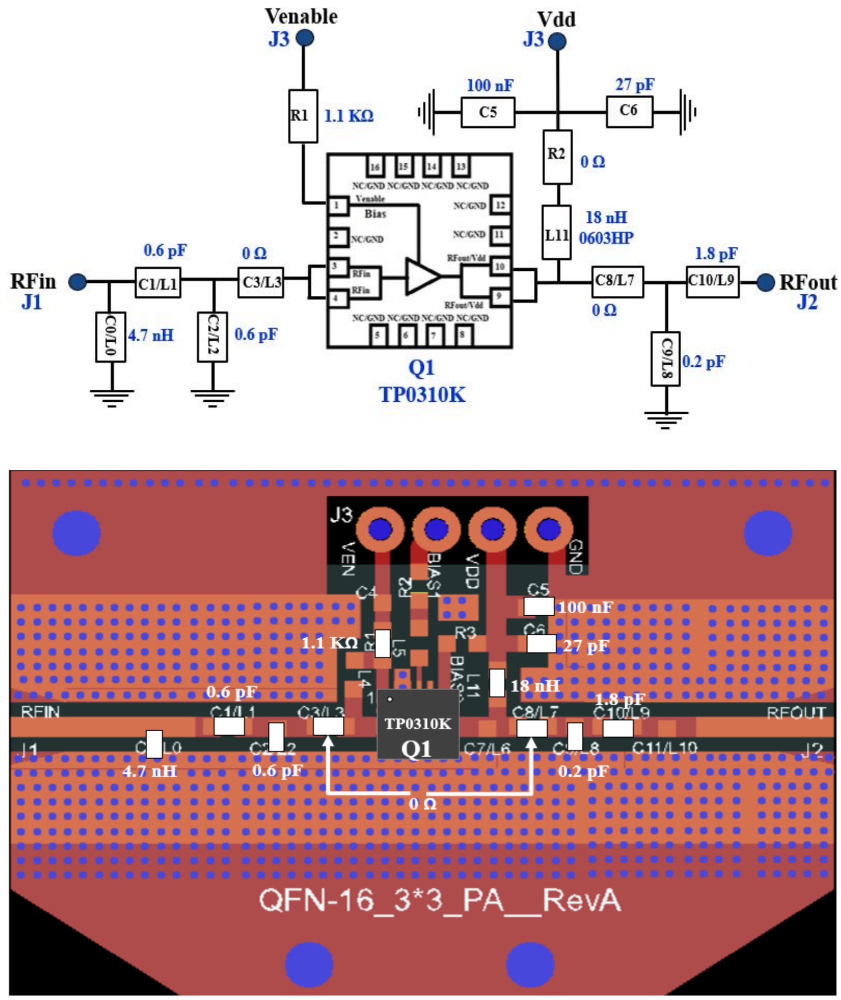
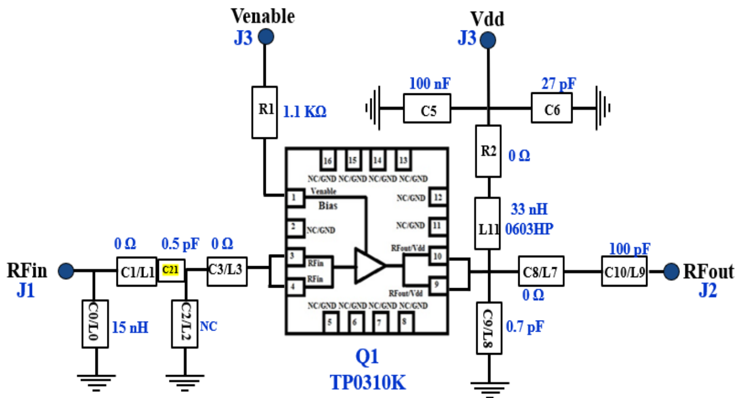


Figure 11.2 Schematic & Layout of the 2500 – 2700 MHz EVB B

Table 11.2 BOM of the 2500 – 2700 MHz EVB B

Component ID	Value	Manufacturer	Recommended Part Number
C0/L0	4.7 nH	Coil craft	0402HP-4N7XGRW
C1/L1, C2/L2	0.6 pF	Murata	GJM1555C1HR60BB01
C3/L3, C8/L7 & R2	0 Ω	Panasonic	ERJ-2GE0R00X
R1	1.1 KΩ	Panasonic	ERJ-2RKF1101X
C9/L8	0.2 pF	Murata	GJM1555C1HR20BB01
C10/L9	1.8 pF	Murata	GJM1555C1H1R8BB01
L11	18 nH	Coil craft	0402HP-18NXGRW
C5	100 nF	TDK	C1005X7R1H104K050BE
C6	27 pF	Murata	GJM1555C1H270JB01D
Q1	GaAs LNA	Tagore Tech	TP0310K
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

11.3 3300 – 3800 MHz EVB C



An external series cut has been made between M1and M2 in the EVB board to incorporated an extra series capacitance 0.5 pF(named as C21) at the input side match.

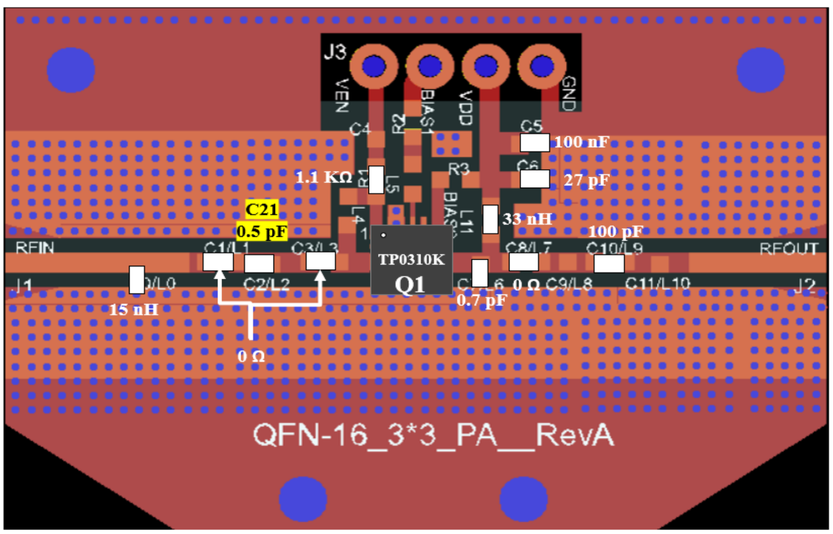


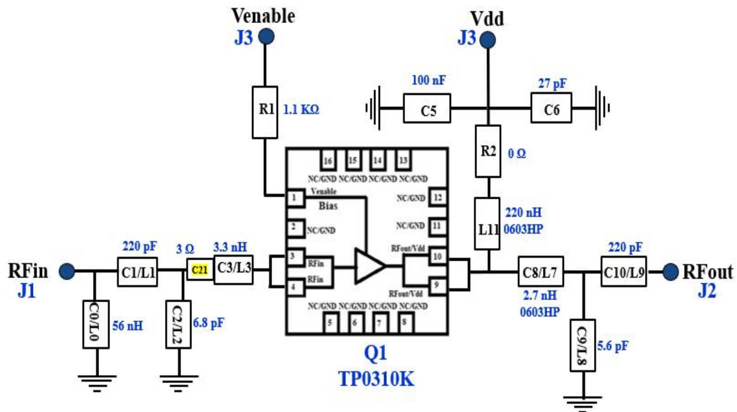
Figure 11.3 Schematic & Layout of the 3300 – 3800 MHz EVB C

Note: An external series cut has been made between C1/L1 and C2/L2 in the EVB board to incorporate an extra series capacitance 0.5 pF (named as C21) at the input side match.

Table 11.3 BOM of the 3300 – 3800 MHz EVB C

Component ID	Value	Manufacturer	Recommended Part Number
C0/L0	15 nH	Coil craft	0402HP-15NXGRW
C21	0.5 pF	Murata	GJM1555C1HR50BB01
C1/L1, C3/L3, C8/L7 & R2	0 Ω	Panasonic	ERJ-2GE0R00X
R1	1.1 KΩ	Panasonic	ERJ-2RKF1101X
C7/L6	0.7 pF	Murata	GJM1555C1HR70BB01
C10/L9	100 pF	AVX	04025A101JAT4A
L11	33 nH	Coil craft	0402HP-33NXGRW
C5	100 nF	TDK	C1005X7R1H104K050BE
C6	27 pF	Murata	GJM1555C1H270JB01D
Q1	GaAs LNA	Tagore Tech	TP0310K
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

11.4 130 – 950 MHz EVB D



An external series cut has been made between M2 and M3 in the EVB board to incorporated an extra series resistance (named as C21) at the input side match.

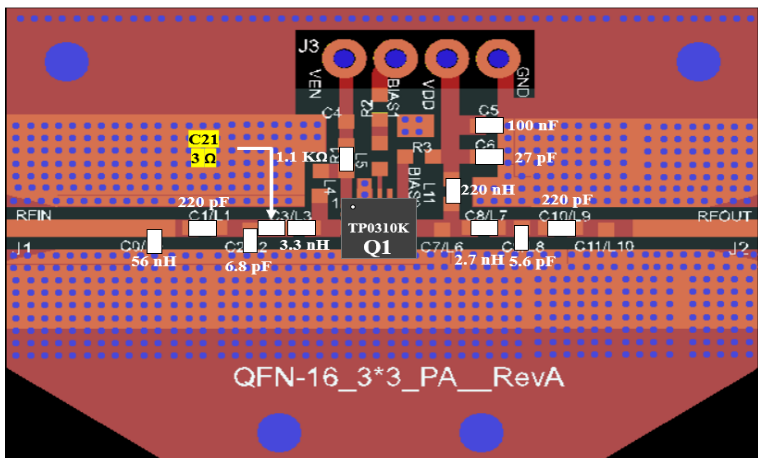


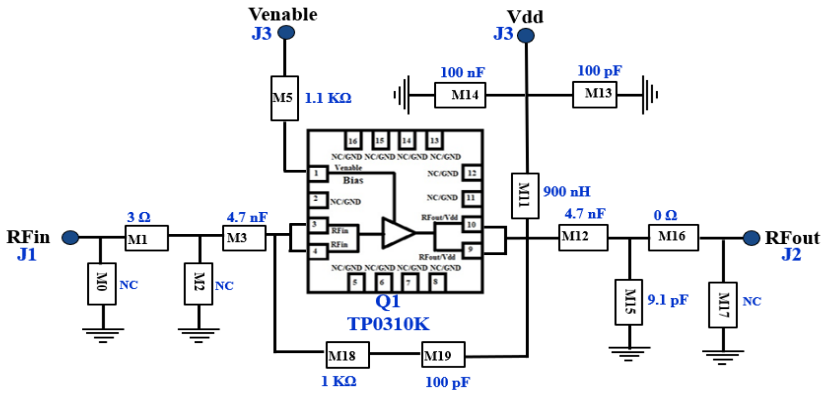
Figure 11.4 Schematic & Layout of the 130 – 950 MHz EVB D

Note: An external series cut has been made between C3/L3 and C2/L2 in the EVB board to incorporate an extra series resistance 3 ohm (named as R14) at the input side match.

Table 11.4 BOM of the 130 – 950 MHz EVB D

Component ID	Value	Manufacturer	Recommended Part Number
C0/L0	56 nH	Coil craft	0402HPH-56NXGLU
C1/L1, C10/L9	220 pF	Murata	GRM0335C1H221FA01D
C2	6.8 pF	Murata	GJM1555C1H6R8BB01D
R14	3 Ω	Panasonic	ERJ-U02F3R00X
C3/L3	3.3 nH	Coil craft	0402HP-3N3XGLU
R1	1.1 kΩ	Panasonic	ERJ-2RKF1101X
C5	100 nF	TDK	C1005X7R1H104K050BE
C6	27 pF	Murata	GJM1555C1H270JB01D
L11	220 nH	Coil craft	0402HPH-R22XGLU
C8/L7	2.7 nH	Coil craft	0402HP-2N7XGLU
C9/L8	5.6 pF	Murata	GJM1555C1H5R6BB01D
Q1	GaAs Power LNA	Tagore Tech	TP0310K
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

11.5 30 – 525 MHz EVB E



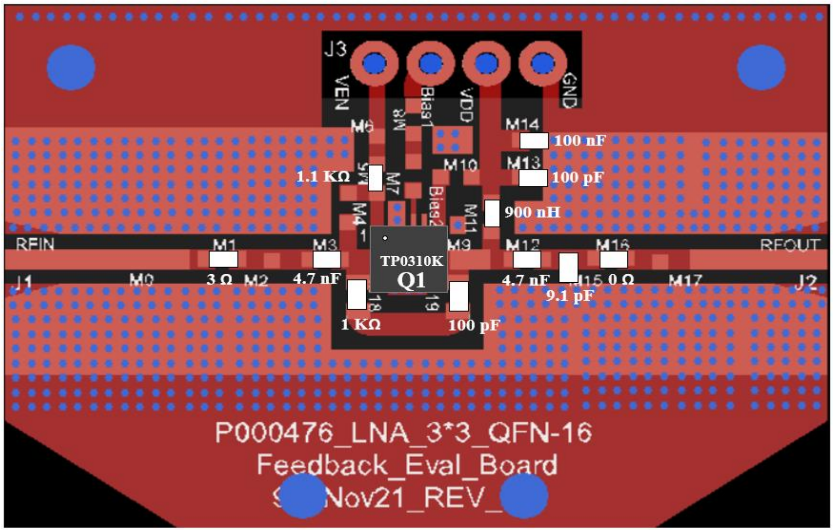


Figure 11.5 Schematic & Layout of the 30 – 525 MHz EVB E

Table 11.5 BOM of the 30 – 525 MHz EVB E

Component ID	Value	Manufacturer	Recommended Part Number
M1	3 Ω	Panasonic	ERJ-U02F3R00X
M3, M12	4.7 nF	Murata	GRM1885C1H472JA01D
M5	1.1 KΩ	Panasonic	ERJ-2RKF1101X
M11	900 nH	Coil craft	1008AF-901XJLC
M13, M19	100 pF	AVX	04025A101JAT4A
M14	100 nF	TDK	C1005X7R1H104K050BE
M15	9.1 pF	Murata	GJM1555C1H9R1BB01
M16	0 Ω	Panasonic	ERJ-2GE0R00X
M18	1.0 KΩ	Panasonic	ERJ-2RKF1001X
Q1	GaAs Power LNA	Tagore Tech	TP0310K
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

11.6 2900 – 3500 MHz EVB F

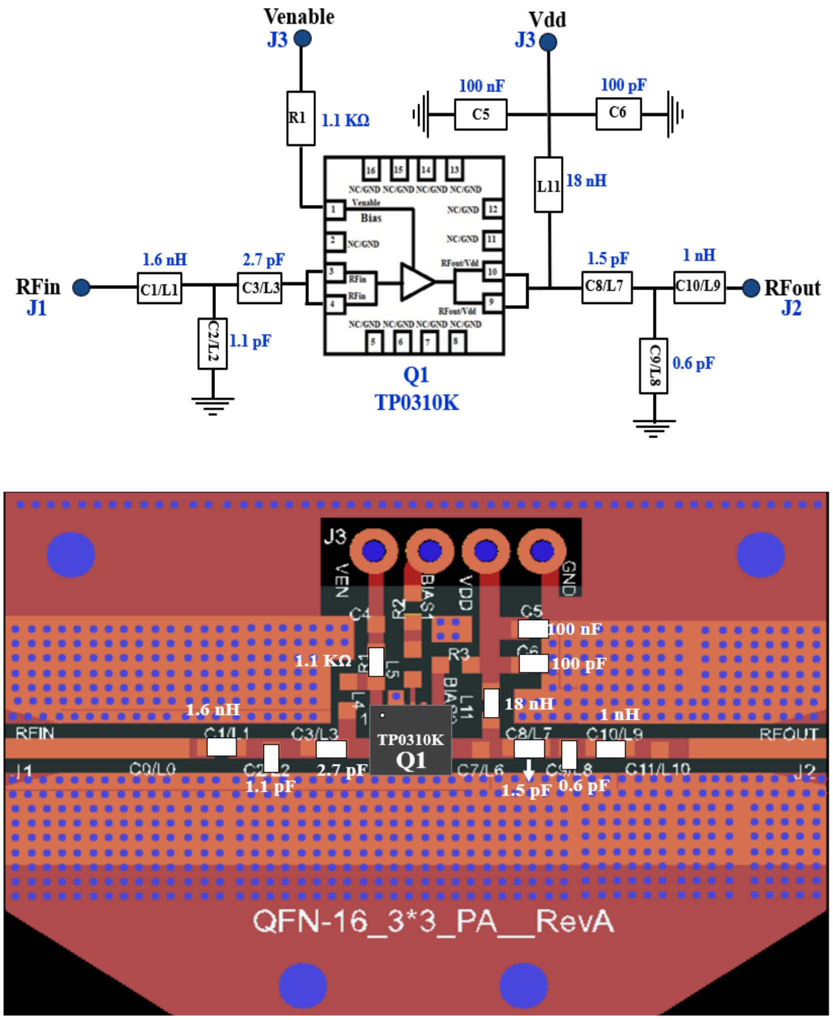


Figure 11.6 Schematic & Layout of the 2900 – 3500 MHz EVB F

Table 11.6 BOM of the 2900 – 3500 MHz EVB F

Component ID	Value	Manufacturer	Recommended Part Number
L1	1.6 nH	Coil craft	0603HC-1N6XJRW
C2	1.1 pF	AVX	600S1R1BT250XT
C3	2.7 pF	AVX	600S2R7BT250XT
R1	1.1 KΩ	Panasonic	ERJ-2RKF1111X
C5	100 nF	TDK	C1005X7R1H104K050BE
C6	100 pF	AVX	04025A101JAT4A
C8	1.5 pF	AVX	600S1R5BT250XT
C9	0.6 pF	AVX	600S0R6BT250XT
L9	1 nH	Coil craft	0402HP-1N0XJRW
L11	18 nH	Coil craft	0402HP-18NXGRW
Q1	GaAs Power LNA	Tagore Tech	TP0310K
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

12.0 Test Procedures

Biasing Sequence

To properly bias the TP0310K-EVB-A, follow these steps:
Connect the supply Ground the Ground test point.

- Apply bias to the Venable=5 V test points.
- Apply bias to the Vdd=5 V test point.
- Apply an RF input signal.

The TP0310K-EVB-A is shipped fully assembled and tested. Figure 12.1 illustrates a basic test setup diagram for evaluating s-parameters, which includes gain, input output return loss and reverse isolation using a network analyzer. Follow these steps to complete the test setup and verify the operation of the TP0310K-EVB-A

1. Connect the Ground test point to the ground terminal of the power supply.
2. Connect the Venable and Vdd test points to the voltage output terminal of a 5 V supply that sources a current of approximately 140 mA.
3. Connect a calibrated network analyzer to the RF-in, and RF-out SMA connectors. Sweep the frequency from 1 GHz to 6 GHz and set the power to -25 dBm.

The TP0310K-EVB-A is expected to have a gain of 16.5 dB at 1.8 GHz. Refer to Table 9.1 for the expected results.
Additional test equipment is required for a comprehensive evaluation of the device's functions and performance.
For noise figure evaluation, use either a noise figure analyzer or a spectrum analyzer with a noise option. It is recommended to use a low excess noise ratio (ENR) noise source.
For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is recommended.
For power compression and power handling evaluations, use a two-channel power meter and a signal generator. Ensure that the input power amplifier has sufficient power capacity. Test accessories such as couplers and attenuators must also have adequate power handling capabilities.

Please note that measurements conducted at the SMA connectors of the TP0310K-EVB-A include the losses of the SMA connectors and the PCB. The through line should be measured to calibrate the effects of the TP0310K-EVB-A. The through line consists of an RF input line and an RF output line that are connected to the device and have equal lengths.

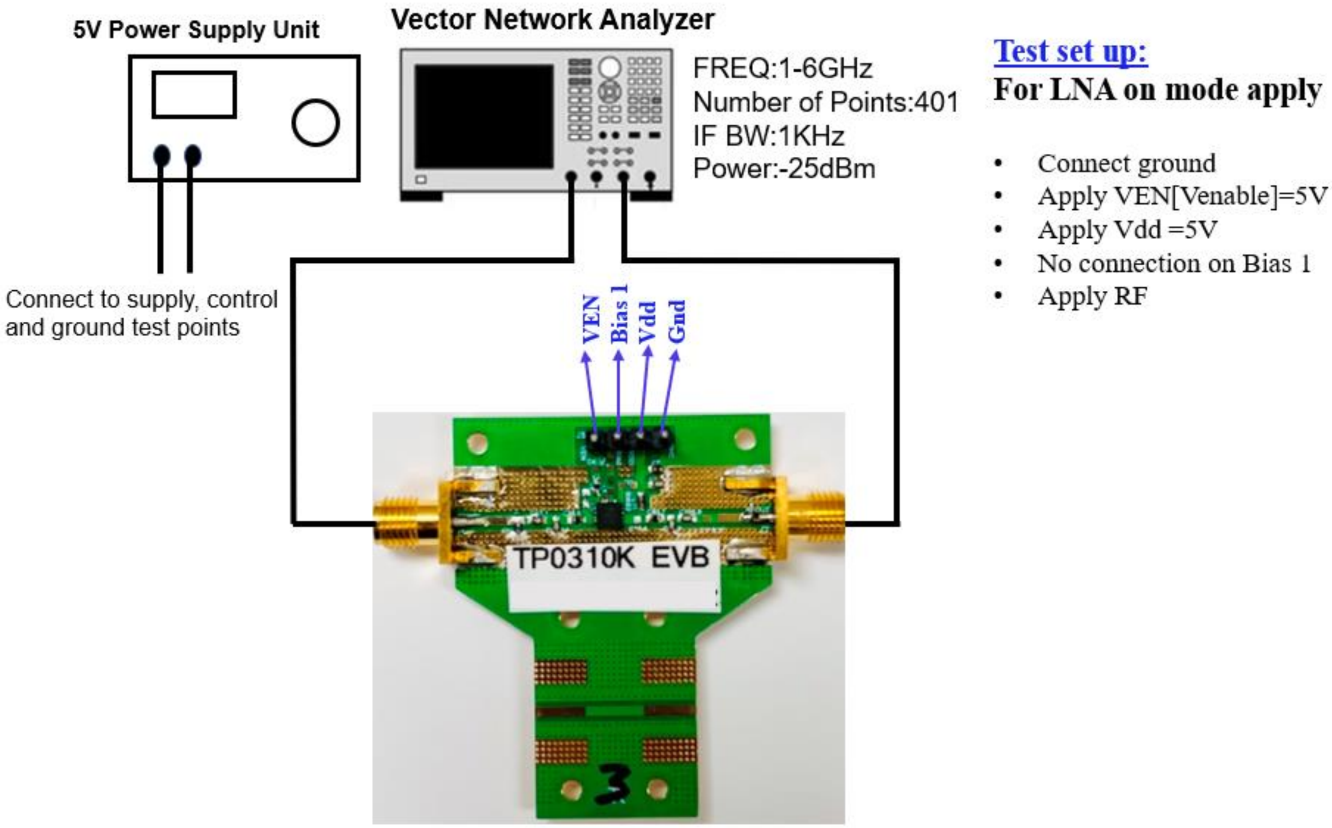


Figure 12.1 TEST Set Up Diagram

13.0 Device Package Information

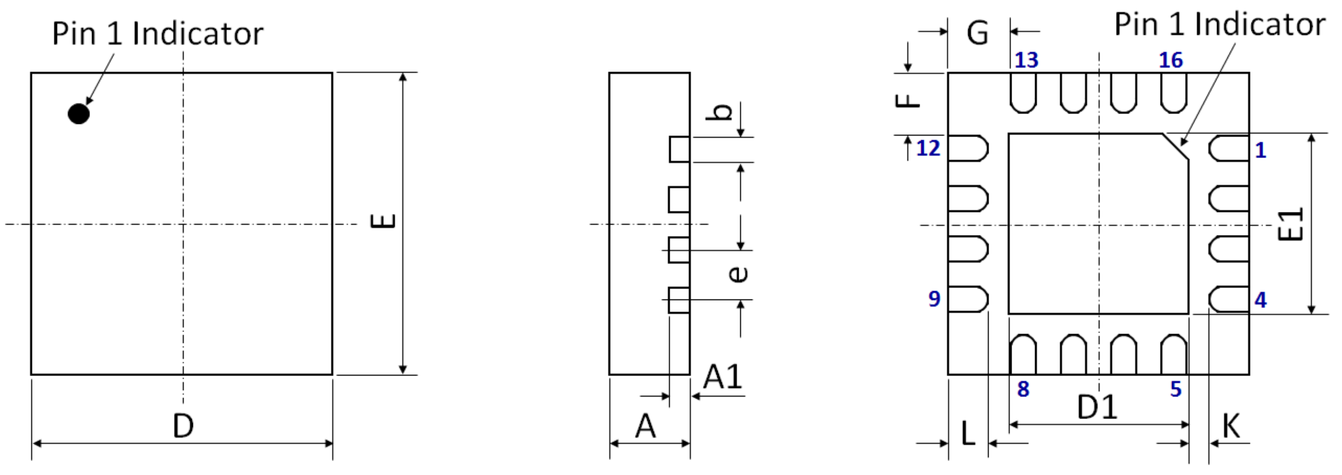


Figure 13.1 Device Package Drawing
(All dimensions are in mm)

Table 13.1 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.80	±0.05	E	3.00 BSC	±0.05
A1	0.203	±0.02	E1	1.70	±0.05
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	3.00 BSC	±0.05	G	0.625	±0.05
D1	1.70	±0.05	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5 μm ~ 20 μm (Typical 10 μm ~ 12 μm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

14.0 PCB Land Design

Guidelines:
[1] 2-layer PCB is recommended.
[2] Via diameter is recommended to be 0.3 mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad and should be filled/plugged with solder or copper.
[4] The maximum via number for the center pad is 3(X)×3(Y)=9

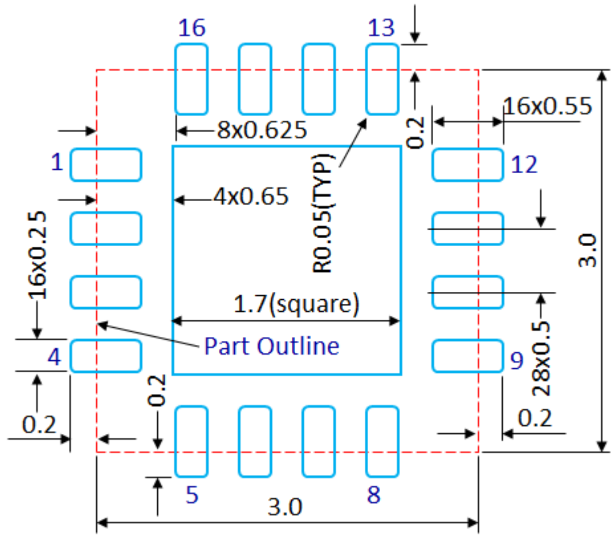


Figure 14.1 PCB Land Pattern
(Dimensions are in mm)

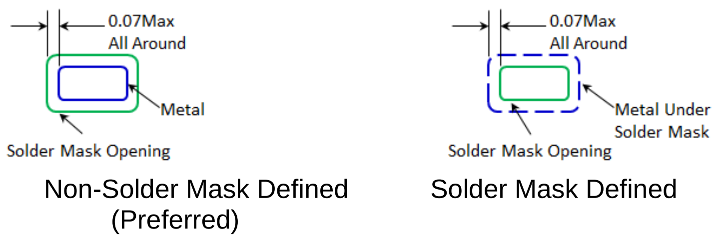


Figure 14.2 Solder Mask Pattern
(Dimensions are in mm)

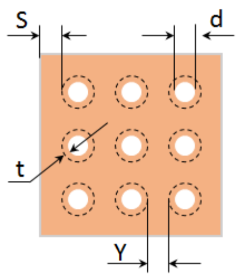


Figure 14.3 Thermal Via Pattern
(Recommended Values: S≥0.15 mm; Y≥0.20 mm; d=0.3 mm; Plating Thickness t=25 μm or 50 μm)

15.0 PCB Stencil Design

Guidelines:
[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
[2] Stencil thickness is recommended to be 125 μm.

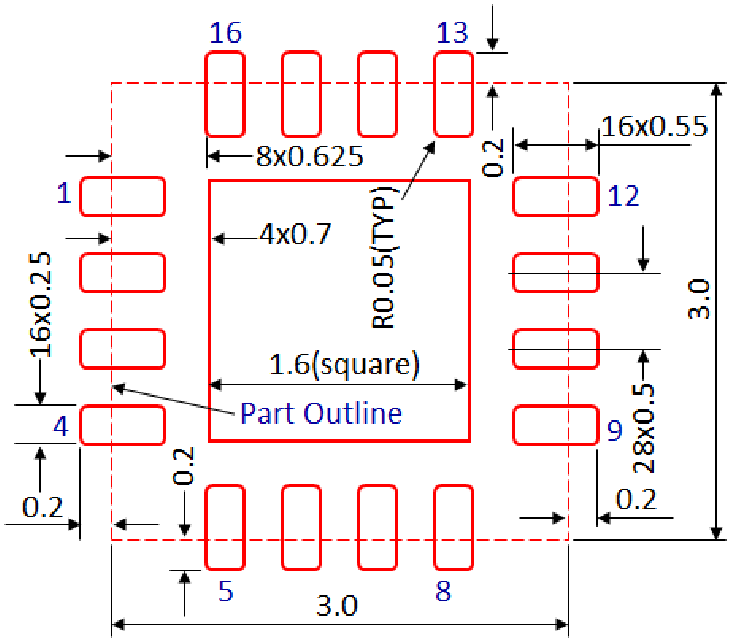


Figure 15.1 Stencil Openings
(Dimensions are in mm)

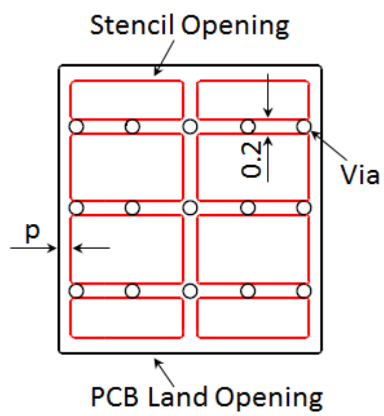


Figure 15.2 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

16.0 Tape and Reel Information

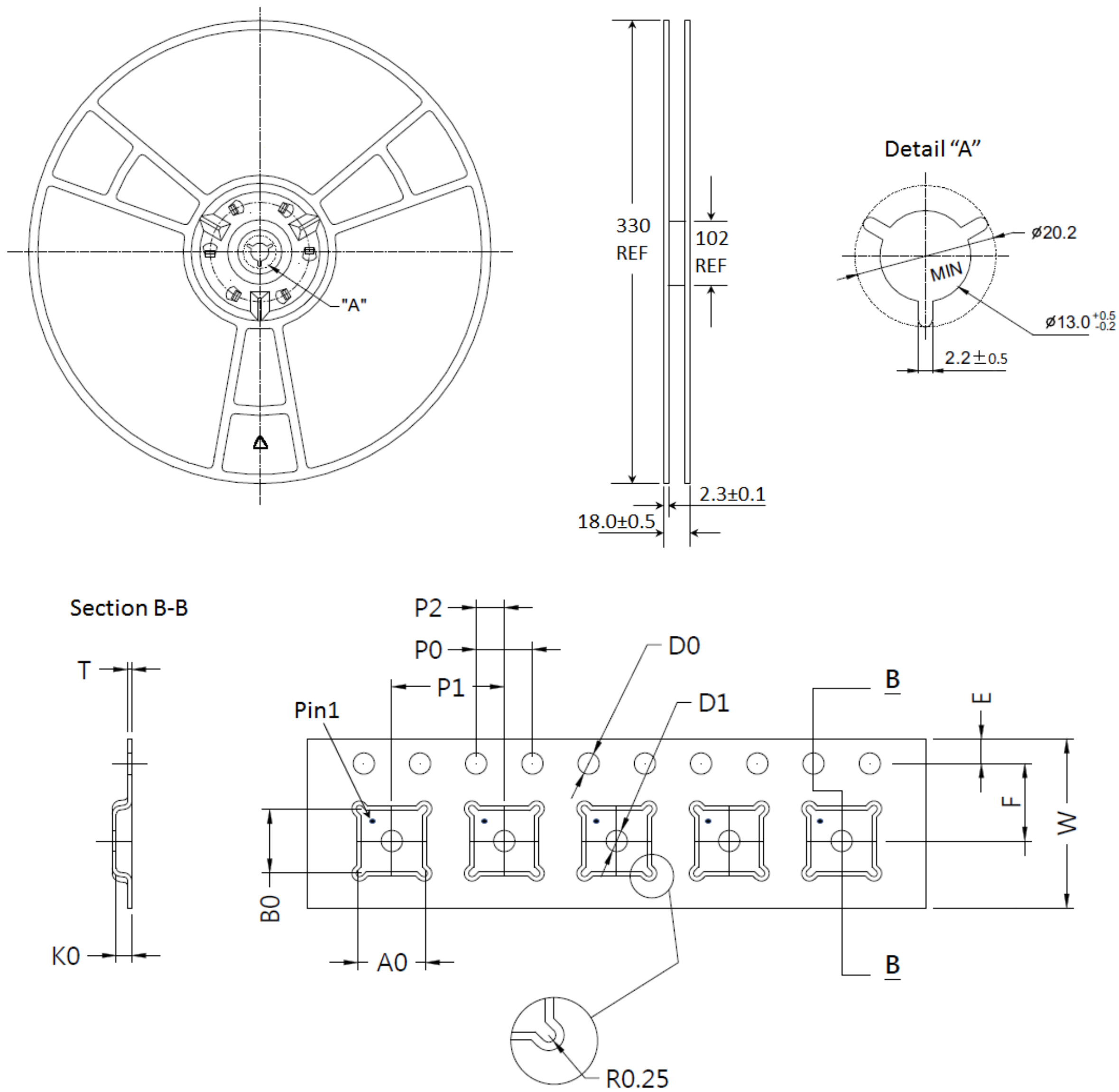


Figure 16.1 Tape and Reel Drawing

Table 16.1 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	3.35	±0.10	K0	1.10	±0.10
B0	3.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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