4T/5T Binary Shunt Tuning Switch, R_{ON}=0.5/1/2 Ω, V_{PEAK}=100 V

Features

- Fully integrated solution, single V_{DD} = 2.6 V – 5.25 V
- Frequency Range 1 MHz to 1000 MHz
- Five throws: R_{ON} = 3 × 0.5 Ω, 1 Ω, 2 Ω
- Binary weighted 4T: 0.25 Ω, 0.5 Ω, 1 Ω, 2 Ω
- Throws grounded inside the package
- V_{PEAK} = 100 V
- Highest pulse power in the industry
- No sudden voltage breakdown compared to SOI
- Switch time = 7.6 μs, no power derating
- Low power consumption, less than 1 mW
- No need to supply negative voltages

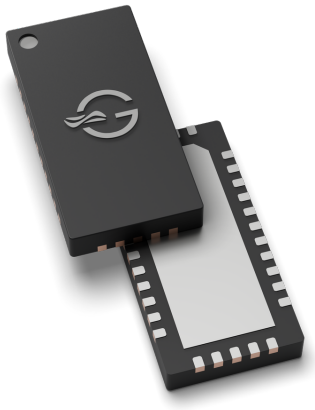


Figure 1: TS63562D in 6.0 x 3.0 mm^2 QFN 32-pin package.

Applications

- Tactical radio
- Tunable filters
- Antenna tuning
- Medical - Ultrasound
- Medical - MRI

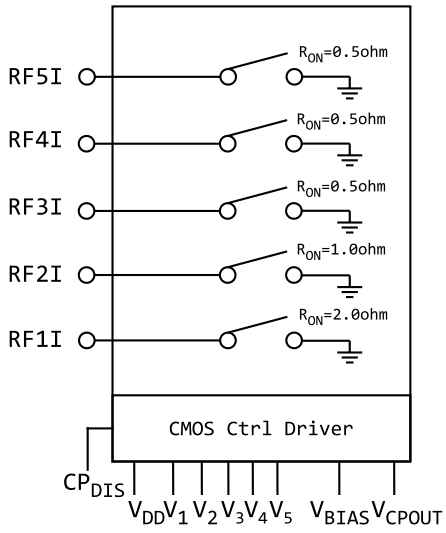


Figure 2: TS63562D functional diagram

General Description

The TS63562D is a fully integrated 5-throw (5T) binary shunt tuning switch based on GaN technology, designed for high power tunable antenna and filter applications in the HF, VHF, UHF, and L bands. Covering 1 MHz to 1 GHz, it has three throws with $R_{ON} = 0.5\,\Omega$, one with 1 Ω and one with 2 Ω; with two 0.5 Ω throws in parallel it is a binary weighted 4-throw switch (0.25 / 0.5 / 1 / 2 Ω) for constant-Q capacitor banks. The TS63562D is the TS63560D with the outputs of the five throws bonded to the ground pad inside the package: each throw switches its RFxI pin to ground with a short, low-inductance ground connection. The peak voltage capability is 100 V. The TS63562D operates from a single standard V_{DD} supply; no external negative or high voltages are required, as bias generation is fully integrated.

The TS63562D is housed in a compact 6.0×3.0 mm^2 32-lead Quad Flat No-lead (QFN) plastic package.

RoHS

RoHS10/REACH/Halogen free

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Ordering information

Table 1: Ordering Information

Device Part Number	Package Type	Notes
TS63562D	32 Pin 6.0x3.0x0.75 mm^3 QFN	Core part number
TS63562D-EVB	Evaluation Board	
TS63562DMTRPBF[1]	330 mm reel, 3 000 pcs	Full reel

[1] MTRPBF - M: Manufacturing, TR: Tape and Reel, and PBF: lead free.

Table 2: Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3 000	13” (330mm)	18mm

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Pin Assignment

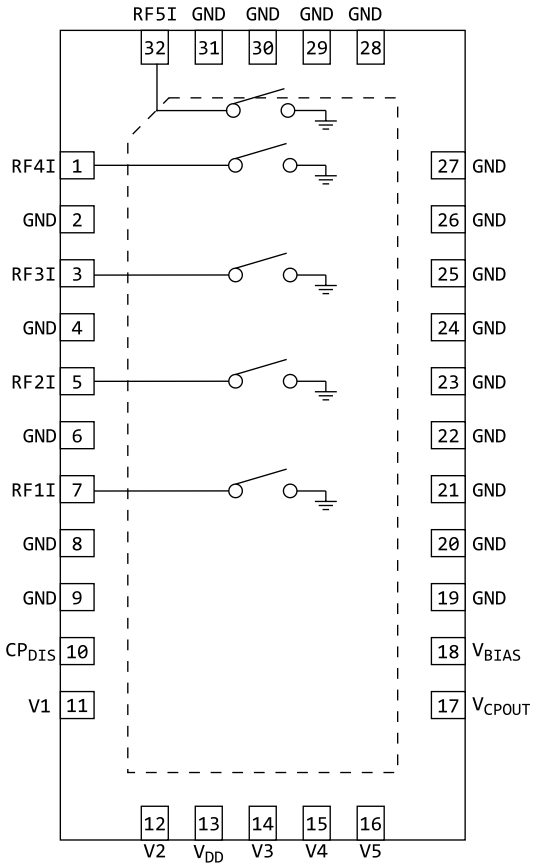


Figure 3: TS63562D pin assignment [top view]

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Table 3: Pin Definition

Pin Number	Pin Name	Description
32	$\mathrm{RF5I}$	RF port 5, throw 5 to ground, $R_{\mathrm{ON}} = 0.5\,\Omega$
1	$\mathrm{RF4I}$	RF port 4, throw 4 to ground, $R_{\mathrm{ON}} = 0.5\,\Omega$
3	$\mathrm{RF3I}$	RF port 3, throw 3 to ground, $R_{\mathrm{ON}} = 0.5\,\Omega$
5	$\mathrm{RF2I}$	RF port 2, throw 2 to ground, $R_{\mathrm{ON}} = 1\,\Omega$
7	$\mathrm{RF1I}$	RF port 1, throw 1 to ground, $R_{\mathrm{ON}} = 2\,\Omega$
18	$\mathrm{V_{BIAS}}$	Bias voltage input, -18 V...-20 V, either from external source or internal charge pump
17	$\mathrm{V_{CPOUT}}$	Internal charge pump voltage output.
13	$\mathrm{V_{DD}}$	DC Power Supply
10	$\mathrm{CP_{DIS}}$	Disable Internal Charge Pump[3]
11	$\mathrm{V_1}$	Switch control input 1 ($\mathrm{RF1I - GND}$)
12	$\mathrm{V_2}$	Switch control input 2 ($\mathrm{RF2I - GND}$)
14	$\mathrm{V_3}$	Switch control input 3 ($\mathrm{RF3I - GND}$)
15	$\mathrm{V_4}$	Switch control input 4 ($\mathrm{RF4I - GND}$)
16	$\mathrm{V_5}$	Switch control input 5 ($\mathrm{RF5I - GND}$)
2,4,6,8,9,19,20,21,22, 23,24,25,26,27,28,29,30,31	GND	Connect to ground[2]
33 [1]	GND	Ground thermal pad, please connect to GND

[1] The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias, and adequate heat sinking must be used to ensure proper operation and thermal management.
[2] These pins are NC pins inside the package (pins 21, 23, 25, 27 and 28 are the RF outputs of the TS63560D; on the TS63562D the throw outputs are bonded to the ground pad). To avoid floating pins around RF lines, we request these to be connected to ground.
[3] Feeding $\mathrm{V_{DD}}$ to this pin disables the internal charge pump. In this case, ground $\mathrm{V_{CPOUT}}$ and feed -18 V...-20 V to $\mathrm{V_{BIAS}}$.

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Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings $T_A = +25$°C unless otherwise specified[1].

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	V_{DD}	5.5	V
Storage Temperature Range	T_{st}	−55 – 125	°C
Operating Temperature Range	T_{op}	−40 – 85	°C
Maximum Junction Temperature	T_j	+140	°C
Maximum RF CW input power	RFxI	tbd	dBm
Maximum RF peak input power, 1% duty cycle, 10μs pulse	RFxI	tbd	dBm
Maximum RF peak voltage	RFxI	tbd	V
Maximum (min) bias voltage	V_{BIAS}	-21	V
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta jc}$	tbd	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta jt}$	tbd	°C/W
Soldering Temperature	T_{solder}	+260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 – $<$1000	V
Charged Device Model (CDM)	Level C3	$\geq$1000	V
Moisture Rating			
Moisture Sensitivity Level[2]	MSL	1	

[1] Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and can cause permanent damage to the device. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit. Functional operation of the device is not implied in any conditions above those indicated in the Electrical Specifications section.

[2] Tagore recommends to store parts in moisture barrier bags to preserve solderability.

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Electrical Specifications

Table 5: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	1		1000	MHz
ON Resistance	RF3, RF4, RF5		0.50		Ω
R_{ON}	RF2		1.0		Ω
	RF1		2.0		Ω
OFF Resistance	RF3, RF4, RF5		250		kΩ
R_{OFF}	RF2		500		kΩ
	RF1		1000		kΩ
OFF Capacitance	RF3, RF4, RF5		500		fF
C_{OFF}	RF2		250		fF
	RF1		125		fF
Insertion loss, throw OFF	RF3, RF4, RF5		tbd		dB
RFxI,	RF2		tbd		dB
50 / 500 / 1000 MHz	RF1		tbd		dB
Isolation, throw ON	RF3, RF4, RF5		tbd		dB
RFxI,	RF2		tbd		dB
50 / 500 / 1000 MHz	RF1		tbd		dB
Return Loss, throw OFF	RF3, RF4, RF5		tbd		dB
RFxI,	RF2		tbd		dB
50 / 500 / 1000 MHz	RF1		tbd		dB
Isolation between adjacent	both throws OFF		tbd		dB
throws, RFxI − RFyI	one throw ON		tbd		dB
50 / 500 / 1000 MHz	both throws ON		tbd		dB

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Table 6: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	1		1000	MHz
Harmonic Distortion					
H_2	800 MHz, P_{in} =35 dBm		tbd		dBc
H_3	800 MHz, P_{in} =35 dBm		tbd		dBc
IIP3	800 MHz		tbd		dBm
Power and Compression point					
P_{maxCW}	Max RF CW Power		tbd		dBm
$P_{maxpeak}$	Max RF Peak Power 1% duty cycle		tbd		dBm
Noise					
CP switching noise	RBW=1 kHz		-140		dBm
Switching Time					
t_{ON}[1]	Switch ON time		tbd		μs
t_{OFF}[1]	Switch OFF time		7.6		μs
t_{RISE}	Switch RISE time		tbd		μs
t_{FALL}	Switch FALL time		tbd		μs
$t_{startup}$, $C_{VCP} = 1$ nF	Start-up time		0.8		ms
Power Supply, DC					
Control voltage	Power Supply V_{DD}	2.6	3.3	5.25	V
	All control pins high[3], V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3	0	0.5	V
Bias voltage[2]	Bias pin, V_{BIAS}	-20		-18	V
Control current	All control pins high, I_{ih}			7.5	μA
	All control pins low, I_{il}		0		μA
Current consumption	I_{DD}, active mode (V_{DD} on)		220		μA

[1] This switching time is complete switching time. Many industry solutions require external biasing and control circuitry, which is not taken into account in switching time. TS63562D switching time definition includes time of the internal biasing and control circuitry.
[2] Bias voltage can be fed externally, or use internal charge pump. Internal charge pump produces -18 V. Please connect output of internal charge pump V_{CPOUT} to V_{BIAS} and connect CP_{DIS} to GND.
[3] Control voltage V_{ih} cannot be higher than V_{DD} (to avoid forward biasing of ESD diode).

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Switch Control and Internal charge pump

Table 7: Switch Control Table

V_{DD}[1]	V_5	V_4	V_3	V_2	V_1	**Switch state**[2]
1	x	x	x	x	1	RF1I – GND ON (2 Ω)
1	x	x	x	1	x	RF2I – GND ON (1 Ω)
1	x	x	1	x	x	RF3I – GND ON (0.5 Ω)
1	x	1	x	x	x	RF4I – GND ON (0.5 Ω)
1	1	x	x	x	x	RF5I – GND ON (0.5 Ω)
1	0	0	0	0	0	RFnI – GND ALL RF switch throws OFF
1	1	1	1	1	1	RFnI – GND ALL switch throws are ON, ie. conducting
0	0	0	0	0	0	V_{DD} OFF, RFnI – GND ALL switch throws are ON, ie. conducting

[1] V_{DD} should be applied first before V_1, V_2, V_3, V_4, and V_5, otherwise may cause damage to the device.
[2] x means any state, so all switch throws can be controlled independently.

Internal Charge Pump

TS63562D has an internal charge pump, which can be disabled with the CP_{DIS} pin by connecting it to V_{DD}. Using the internal charge pump, please connect V_{CPOUT} to V_{BIAS} and CP_{DIS} to GND.

As there might be some noise from the charge pump below 250 MHz, it is recommended for frequencies below 250 MHz to disable the charge pump by connecting the CP_{DIS} pin to V_{DD} and to feed -18 V...-20 V to the V_{BIAS} pin. This ensures noise free operation below 250 MHz.

Option 1: Use internal charge pump

- Connect CP_{DIS} pin to GND.
- Connect V_{CPOUT} to V_{BIAS}.

Option 2: Use external negative voltage -18 V...-20 V, charge pump OFF

- Connect CP_{DIS} pin to V_{DD}.
- Connect V_{CPOUT} pin to GND.
- Feed -18 V...-20 V to V_{BIAS} pin.

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Equivalent Circuit Model

Each throw of the TS63562D can be described with the equivalent circuit below, the same model as for the TS63432D. The output of each throw is bonded to the center ground pad inside the package. The bond wires are modelled as series inductances L_{RFI} (to the RFxI pin) and L_{RFO} (to ground, short bond wire), the die pads as $R_{PI} \parallel C_{PI}$ and $R_{PO} \parallel C_{PO}$ to ground, and the switch transistor as a resistor parallel to C_{off} between the die pads. In the off state the resistor is R_{off}, in the on state it is R_{on}. The 1 Ω and 2 Ω throws are scaled from the 0.5 Ω throw: doubling R_{on} doubles R_{off} and halves C_{off}; the bond wires and pads are the same for all throws (Table 8). The model values have been fitted to measurements of the TS63430D in a shunt configuration.

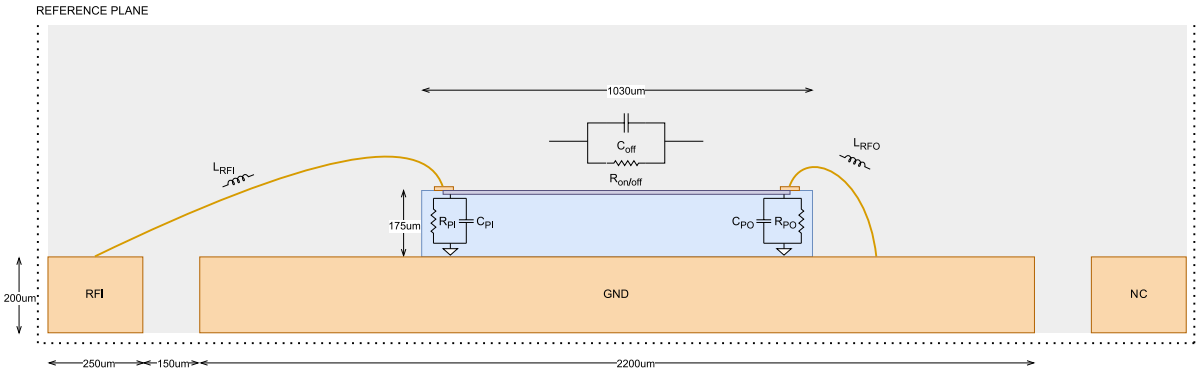


Figure 4: TS63562D cross section of the package with the elements of the equivalent circuit model, one throw.

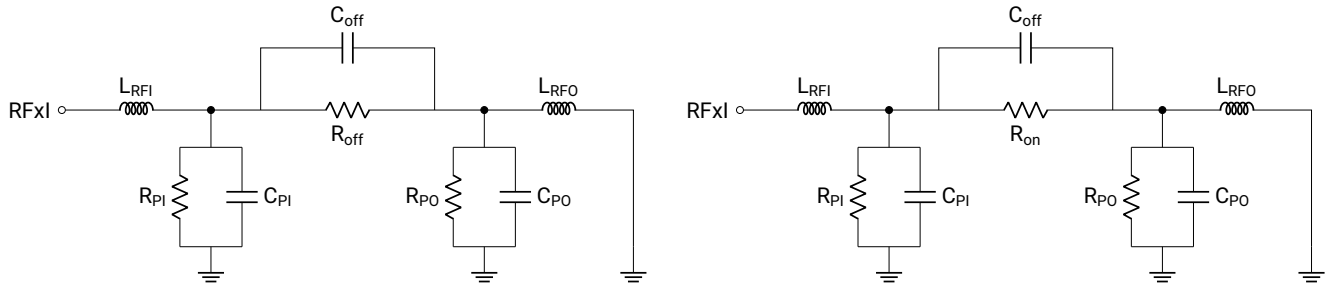


Figure 5: Equivalent circuit model of one throw, RFxI to ground.

Table 8: Equivalent circuit model values per throw.

Element	RF3, RF4, RF5	RF2	RF1
Switch resistance, on state, R_{on}	0.5 Ω	1 Ω	2 Ω
Switch resistance, off state, R_{off}	248.32 kΩ	496.64 kΩ	993.28 kΩ
Switch capacitance, C_{off}	0.3 pF	0.15 pF	0.075 pF
Bond wire, L_{RFI}	0.3 nH	0.3 nH	0.3 nH
Bond wire to the ground pad, L_{RFO}	0.15 nH	0.15 nH	0.15 nH
Pad capacitance, C_{PI}, C_{PO}	0.1 pF	0.1 pF	0.1 pF
Pad resistance, R_{PI}, R_{PO}	78.75 kΩ	78.75 kΩ	78.75 kΩ

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4T Full Binary Weighted Application Example

The TS63562D tuning switch can also be used in a fully binary configuration. This requires the two adjacent 0.5 Ω throws RF4 and RF5 to be connected in parallel (RF4I with RF5I on the PCB, the outputs are grounded inside the package; both controlled together with V_4 and V_5), resulting in $R_{ON} = 0.25\,\Omega$. This is helpful when designing tunable capacitor circuitry with constant Q. Each throw switches a capacitor to ground, so the capacitor and the throw form a series RC circuit, and Q can be written

$$Q = \frac{1}{\omega_0 RC}. \tag{1}$$

Therefore, to have a constant-Q tunable capacitor with binary weighted capacitance values, the switch can be used as a 4T tuning switch with binary weighted series resistance. Assuming that the largest capacitance is connected to the 0.25 Ω throw, we can create for example the following capacitor values:

Table 9: Constant Q Example

RF Port	Capacitance C	Resistance R	RC Product
RF4+RF5	16 pF	0.25 Ω	4 pFΩ
RF3	8 pF	0.50 Ω	4 pFΩ
RF2	4 pF	1.00 Ω	4 pFΩ
RF1	2 pF	2.00 Ω	4 pFΩ

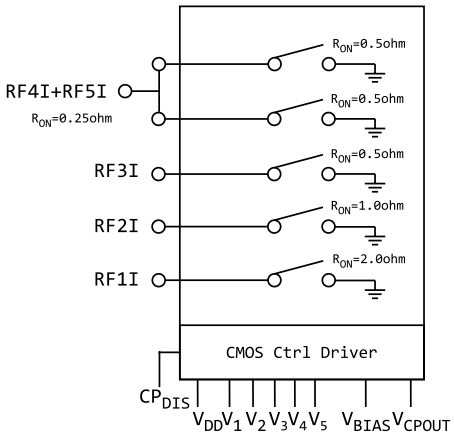


Figure 6: TS63562D functional diagram in Full Binary Weighted 4T configuration.

With this example, one has a 0 stage with a small residual capacitance (the C_{off} of the throws in series with the capacitors) and all values from 2 pF to 30 pF with a step size of 2 pF. The equivalent circuit model values of the four binary throws are given in Table 10.

Table 10: Equivalent circuit model values of the binary weighted throws.

Element	RF4+RF5[1]	RF3	RF2	RF1
R_{on}	0.25 Ω	0.5 Ω	1 Ω	2 Ω
R_{off}	124.16 kΩ	248.32 kΩ	496.64 kΩ	993.28 kΩ
C_{off}	0.6 pF	0.3 pF	0.15 pF	0.075 pF
L_{RFI}	0.15 nH	0.3 nH	0.3 nH	0.3 nH
L_{RFO}	0.075 nH	0.15 nH	0.15 nH	0.15 nH
C_{PI}, C_{PO}	0.2 pF	0.1 pF	0.1 pF	0.1 pF
R_{PI}, R_{PO}	39.375 kΩ	78.75 kΩ	78.75 kΩ	78.75 kΩ

[1] Two 0.5 Ω throws in parallel; the bond wires in parallel without mutual coupling.

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Device Package information

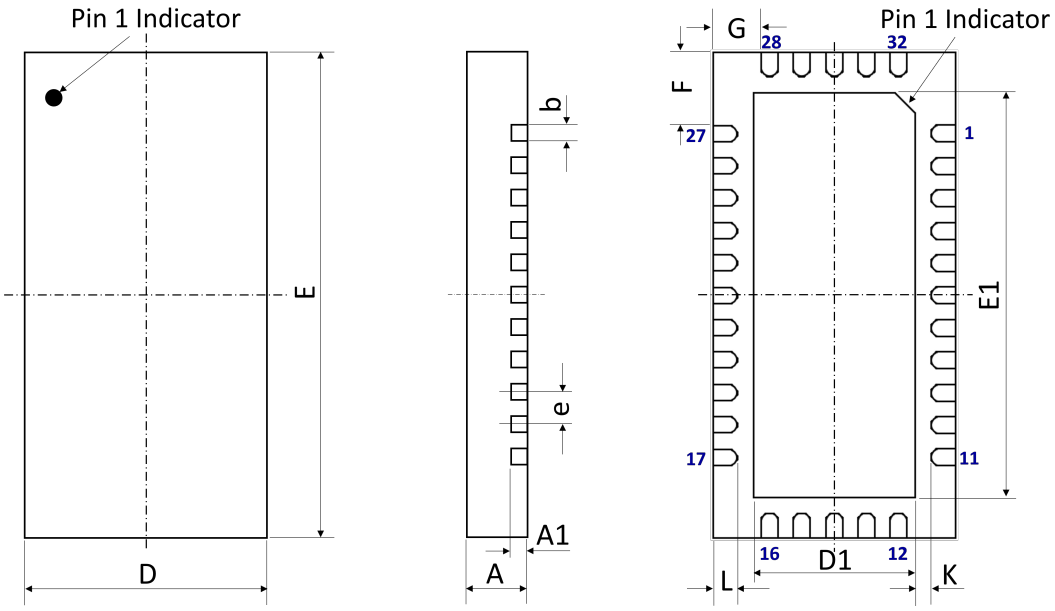
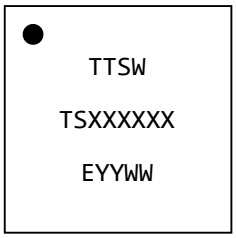


Figure 7: 32-pin QFN 3.0 x 6.0 x 0.75 mm^3 package drawing.

Please refer to application notes TN-001 PCB Design guideline and TN-002 Solder Rework at TagoreTech web page for PCB and soldering guidelines.

Table 11: Device Package Dimensions

Dimension	Value [mm]	Tolerance [mm]	Dimension	Value [mm]	Tolerance [mm]
A	0.75	±0.05	E	6.00 BSC	±0.05
A1	0.203	±0.02	E1	5.00	±0.05
b	0.20	+0.05/-0.07	F	0.90	±0.05
D	3.00 BSC	±0.05	G	0.60	±0.05
D1	2.00	±0.05	L	0.25	±0.05
e	0.40 BSC	±0.05	K	0.25	±0.05



●	Pin 1 indicator
TTSW	TagoreTech SWitch
TSXXXXXX	Part number (8 digits max)
E	Fixed letter before date code
YY	Last two digits of assembly year
WW	Assembly work week

Figure 8: Part marking specification.

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PCB Land Design

Notes:

- 4-layer PCB is recommended.
- Via diameter is recommended to be 0.3mm to prevent solder wicking inside the vias.
- Thermal vias shall only be placed on the center pad.
- The maximum via number for the center pad is 11(X)×11(Y)=121.

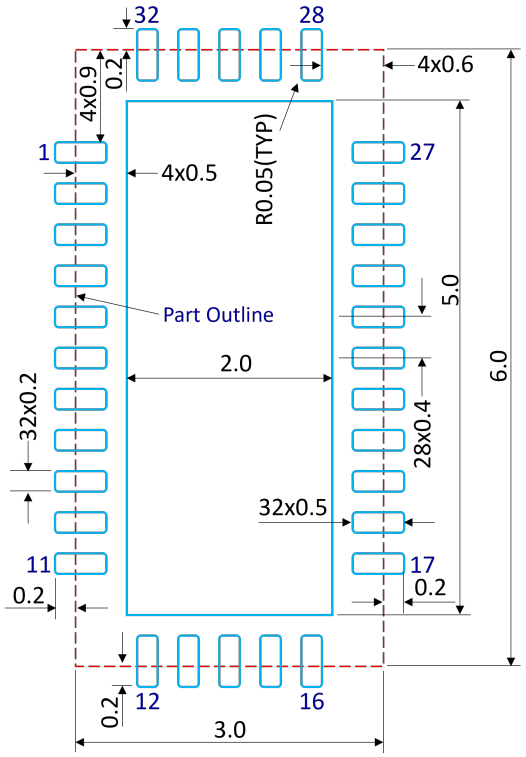


Figure 9: PCB land pattern, dimensions in [mm].

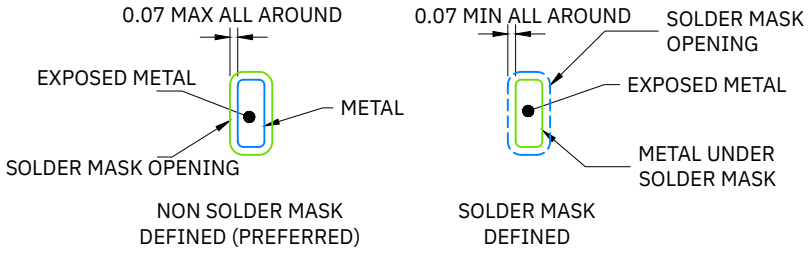


Figure 10: Solder mask opening, dimensions in [mm].

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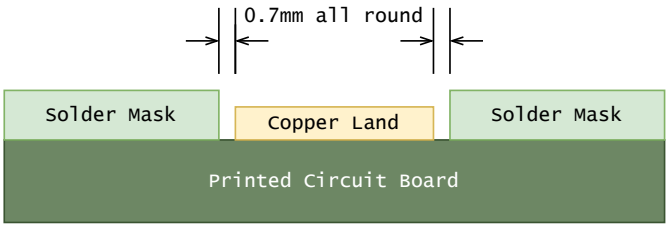


Figure 11: Preferred solder mask opening, side view, dimensions in [mm].

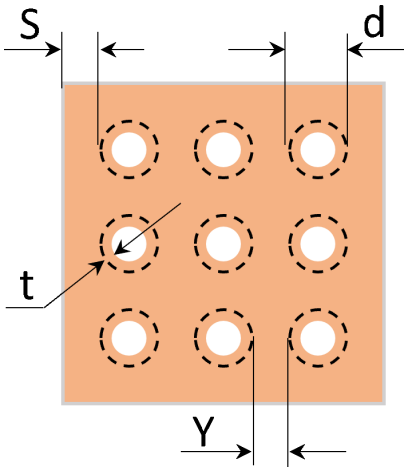


Figure 12: Thermal Via Pattern, Recommended Values: S$\geq$0.15 mm; Y$\geq$0.20 mm; d=0.2 mm; Plating Thickness t=25μm or 50μm.

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PCB Stencil Design

Notes:

- Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- Stencil thickness is recommended to be 125 μm.

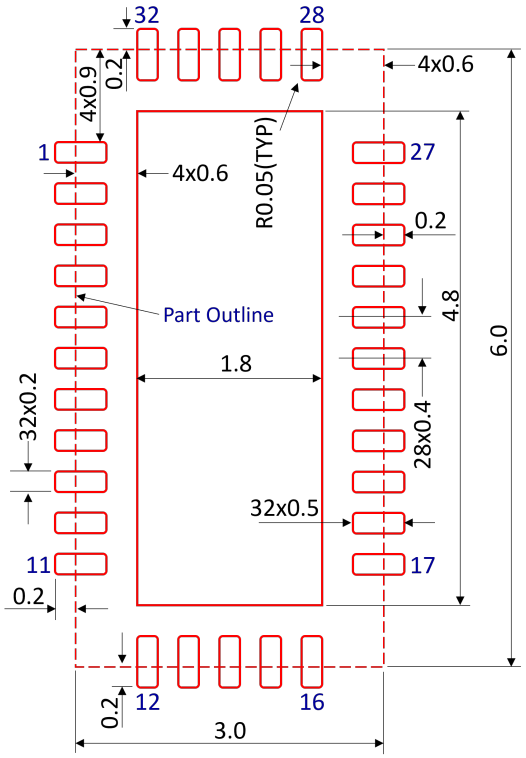


Figure 13: Stencil Openings, dimensions in [mm].

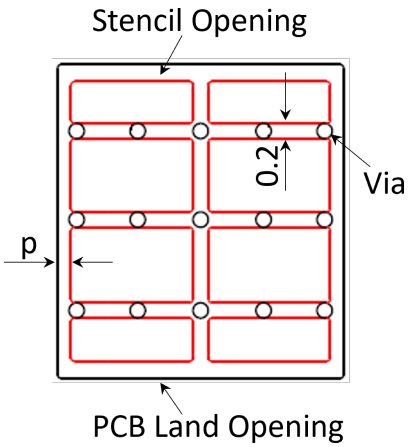
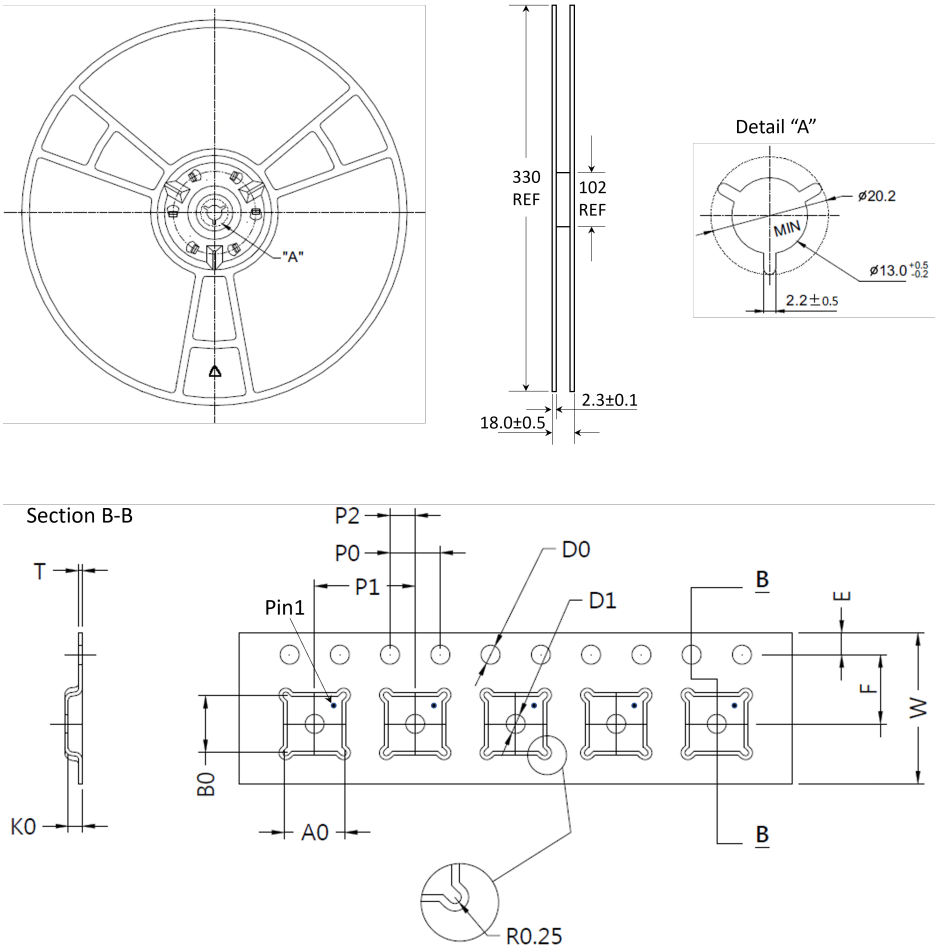


Figure 14: Stencil Openings Shall not Cover Via Areas If Possible, dimensions in [mm].

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Tape and Reel Information



A0[mm]	B0[mm]	D0[mm]	D1[mm]	E[mm]	F[mm]	K0[mm]	P0[mm]	P1[mm]	P2[mm]	T[mm]	W[mm]
3.30	6.30	1.50	1.50	1.75	7.50	1.20	4.00	8.00	2.00	0.30	16.00

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Glossary

IL	Insertion loss
ISO	Isolation
RL	Return loss
VSWR	Voltage Standing Wave Ratio
RFxI	RF port of throw x (x = 1 ...5)
Throw	One shunt switch of the TS63562D, RFxI to ground, controlled by $\mathrm{V_x}$
Binary weighted 4T	RF4 and RF5 in parallel (0.25 Ω), RF3 (0.5 Ω), RF2 (1 Ω), RF1 (2 Ω)
R_{ON}, R_{OFF}, C_{OFF}	On-resistance, off-resistance and off-capacitance of a throw
$\mathrm{V_{BIAS}}$, $\mathrm{V_{CPOUT}}$, $\mathrm{CP_{DIS}}$	Bias voltage input, charge pump output, charge pump disable
EVB	Evaluation board

Changelog

Table 12: Changelog

Date	Revision	Notes
11/07/2026	0.50	Preliminary Datasheet, first publication. Derived from the TS63560D v0.50: outputs of the throws bonded to the center ground pad (shunt throws), pins 21/23/25/27/28 NC, functional diagrams, pin assignment and cross section updated, equivalent circuit model with L_{RFO} 0.15 nH; RF performance tbd.

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