TS7523N - 50W CW GaN Broadband RF Switch SPDT

1.0 Features

- Low insertion loss: 0.30dB @ 500MHz
- High isolation: 47dB @ 500MHz
- High linear power handling capability
- No external DC blocking capacitors on RF lines
- All RF ports OFF state
- Versatile 2.6-5.5V power supply
- Operating frequency: 30MHz to 4.0GHz

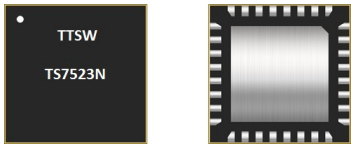


Figure 1 Device Image
(32 Pin 5×5×1.25mm QFN Package)

2.0 Applications

- Private mobile and military radios
- Public safety handsets
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Satellite terminals

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS7523N is a symmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high power switching applications. It is optimized for 30MHz to 4GHz bandwidth providing low insertion loss, high isolation and high linearity within a small package size. TS7523N is an excellent switch for all applications requiring low insertion loss, high isolation and high linearity within a small package size.

The TS7523N is packaged into a compact Quad Flat No lead (QFN) 5x5mm 32 leads plastic package.

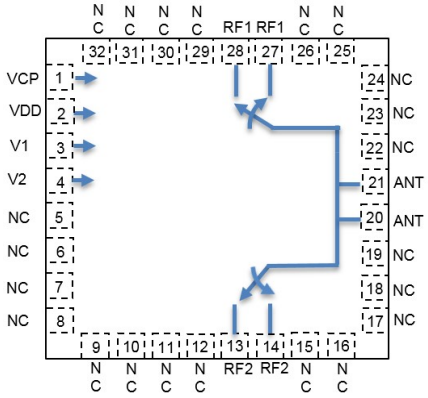


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TS7523N	32 Pin 5×5×0.8mm QFN	Tape and Reel	3000	13” (330mm)	18mm	TS7523NMTRPBF
Evaluation Board						TS7523N-EVB

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	VCP	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time.
2	VDD	DC power supply
3	V1	Switch control input 1
4	V2	Switch control input 2
5,6,7,8,9,10,11,16,17, 18,23,24,25,30,31,32	NC	No internal connection, can be grounded
12,15,19,22,26,29	NC	No internal connection. Do not connect to ground
13,14	RF2	RF port 2
20,21	ANT	Antenna port
27,28	RF1	RF port 1

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias and adequate heat sinking must be used to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	2.6 to 5.5	V
Storage Temperature Range	T_{st}	-55 to +125	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+140	°C
RF Input Power CW, Tcase=+85°C, 800MHz	RFx	47.0	dBm
RF Input Power CW, Tcase=+85°C, 30MHz	RFx	46.0	dBm
RF Input Power (VSWR 20:1), 2 minutes, 800MHz	RFx	45.0	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	7.5	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention: Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+3.3V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency		30		4000	MHz
Insertion loss, RFx	30MHz		0.13		dB
	500MHz		0.16		
	800MHz		0.19		
	4000MHz (matched)		0.39		
Isolation ANT-RFx	30MHz		69		dB
	500MHz		46		
	800MHz		41		
	4000MHz (matched)		21		
Return loss ANT, RFx	30MHz		40		dB
	500MHz		27		
	800MHz		24		
	4000MHz (matched)		24		
Harmonic distortion					
H2	800MHz, Pin=43dBm		-71		dBc
H3	800MHz, Pin=43dBm		-67		dBc
IIP3	800MHz		71		dBm
P0.1dB[1]	0.1dB compression point, 250MHz - 1.5GHz		48		dBm
P0.1dB[1]	0.1dB compression point, 30MHz - <250MHz		47		dBm
Switching time	50% ctrl to 10/90% of the RF value is settled. CP=1nF to ground on VCP pin.		5.2		μs
Control voltage	Power Supply VDD	2.6	3.3	5.5	V
	All control pins high, V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control current	All control pins low, I_{il}		0		μA
	All control pins high, I_{ih}			7.5	μA
Current consumption, IDD	Active mode (VDD on)		180	220	μA

Note:
[1] P0.1dB is a figure of merit.
[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	V2	Active RF Path
0	1	All OFF
0	0	ANT-RF1 ON
1	0	ANT-RF2 ON

Attention:
[1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.
[2] There are internal pull-downs to ground on both V1 and V2 control pins, the state at start-up without any control voltage applied will be ANT-RF1 ON.
[3] If all OFF state is not used, the switch can be operated with single control pin V1.

9.0 Schematic

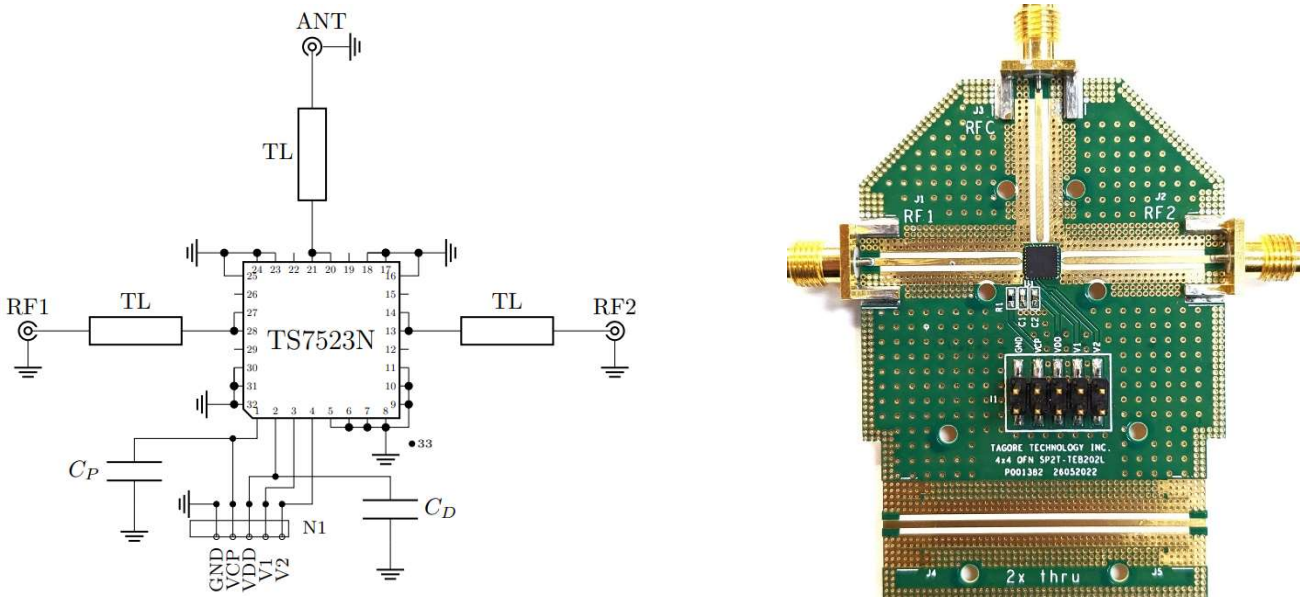


Figure 3 Evaluation Board Schematic

Attention:
[1] 33 refers to the center pad of the device. Multiple Plugged through hole vias should be added on this Ground Pad and adequate heat sinking should be used.
[2] The purpose of connection between VCP and connector N1 is to monitor VCP, do not apply external voltage to VCP.

10.1 Typical Characteristics (unmatched)

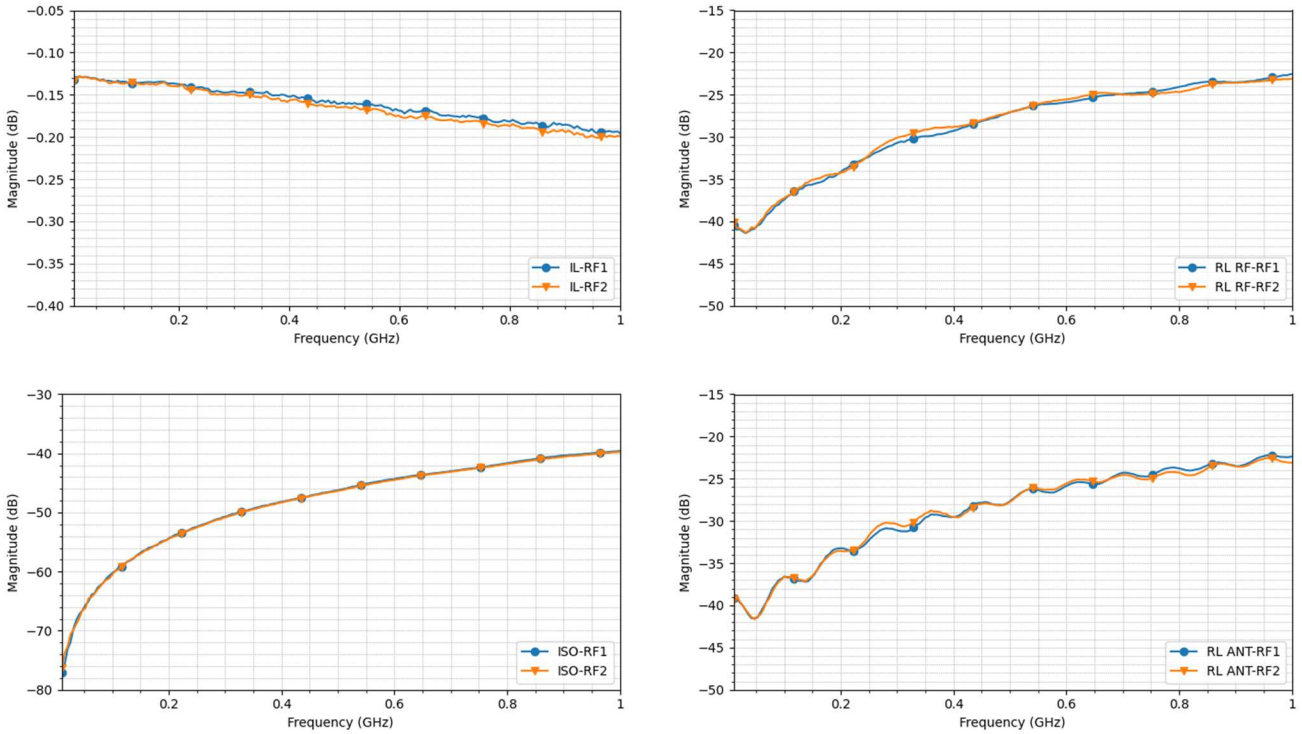


Figure 4.1 Typical Characteristics (unmatched)

10.2 Typical Characteristics (10 MHz – 4000 MHz)

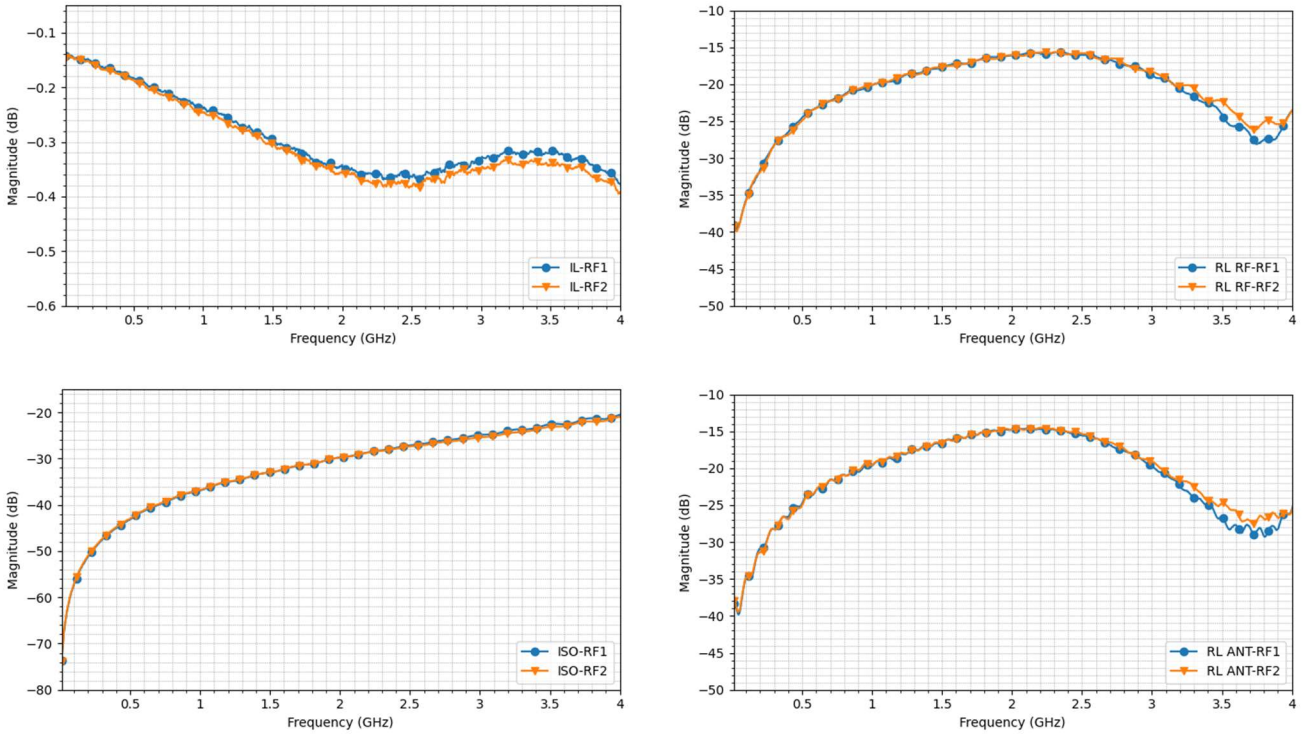


Figure 4.2 Typical Characteristics (10 MHz – 4000 MHz)

11.1 Bill of Materials – (Unmatched)

Table 6.1 Bill of Materials – Unmatched

Component	Part Number	Description	Notes
C_P	GRM155R61E104KA87D	Ceramic capacitor, 0.1 µF, 25 V, ±10%.	
C_D	GRM155R71H103KA88	Ceramic capacitor, 10 nF, 50 V, ±15%.	

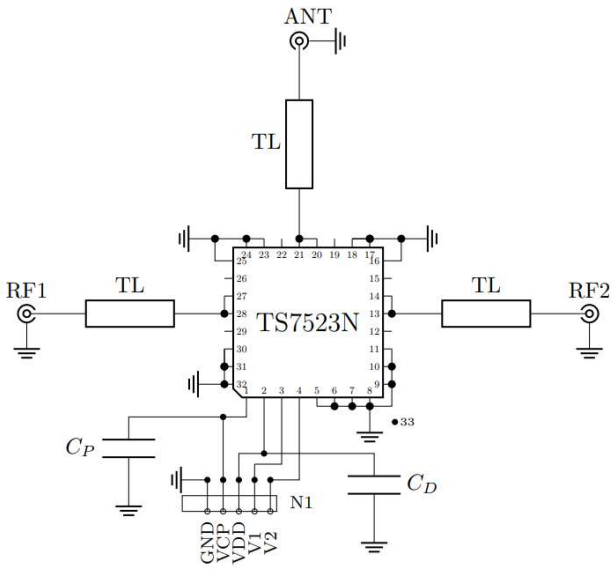


Figure 5.1 Schematic for Unmatched Condition

11.2 Bill of Materials – (10MHz – 4000MHz)

Table 6.2 Bill of Materials – (10MHz – 4000MHz)

Ref	Part Number/Value	Description	Notes
C_P	GRM155R61E104KA87D	Ceramic capacitor, 0.1 µF, 25 V, ±10%.	
C_D	GRM155R71H103KA88	Ceramic capacitor, 10 nF, 50 V, ±15%.	
L_{0a}	0402DC-N80XJRU	Ceramic core chip inductor, 0.8 nH, ± 5%	As close as possible to the switch reference plane.
C_{0a}	0603N0R5BW251	Ceramic capacitor, 0.5 pF, 250V, ± 0.1pF.	

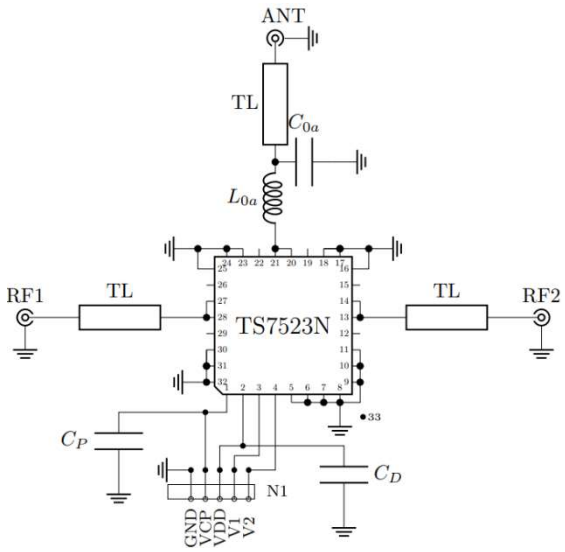


Figure 5.2 Schematic for Matching (10 MHz – 4000MHz)

12.0 Device Package Information

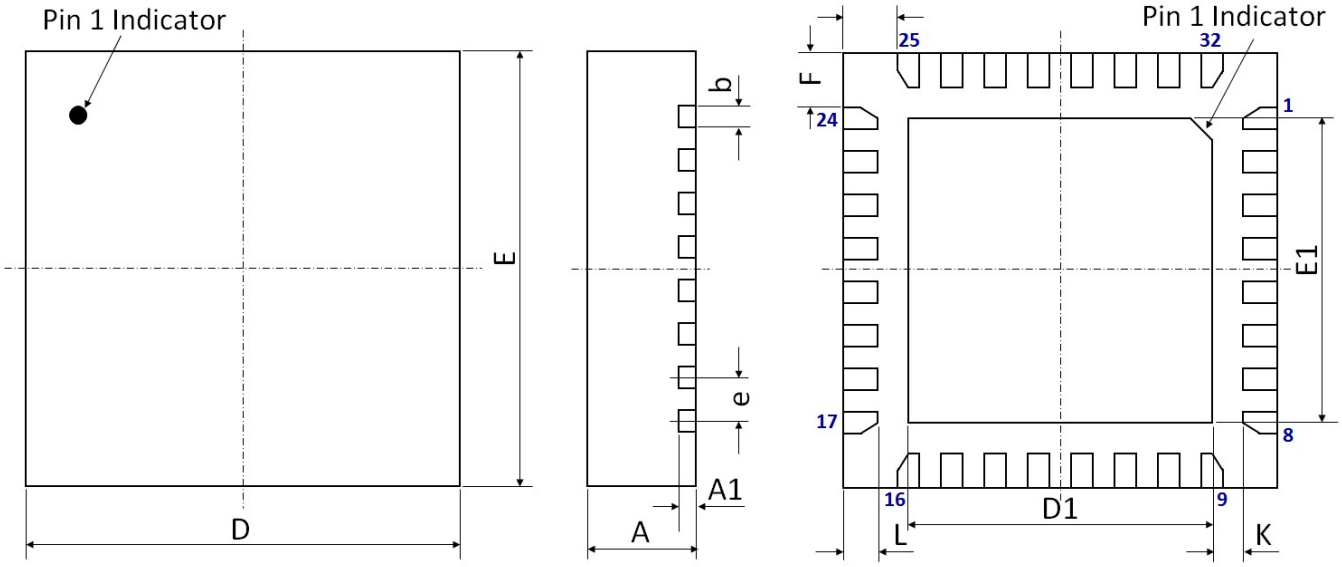


Figure 6 Device Package Drawing
(All dimensions are in mm)

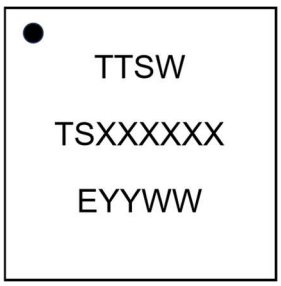
Table 7 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.8	±0.05	E	5.00 BSC	±0.05
A1	0.203	±0.02	E1	3.10	±0.06
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	5.00 BSC	±0.05	G	0.625	±0.05
D1	3.10	±0.06	L	0.40	±0.05
e	0.50 BSC	±0.05	K	0.50	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention:
Please refer to application notes *TN-001* and *TN-003* at http://www.tagoretech.com for PCB and soldering related guidelines.

Top-marking specification:



● = Pin 1 indicator
TTSW = Tagore Technology SWitch
TSXXXXXX = Part number (8 digits max)
E = A fixed letter before the date code
YY = Last two digits of assembly year
WW = Assembly work week

13.0 PCB Land Design

Guidelines:
[1] 4 layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 5(X)×5(Y)=25.

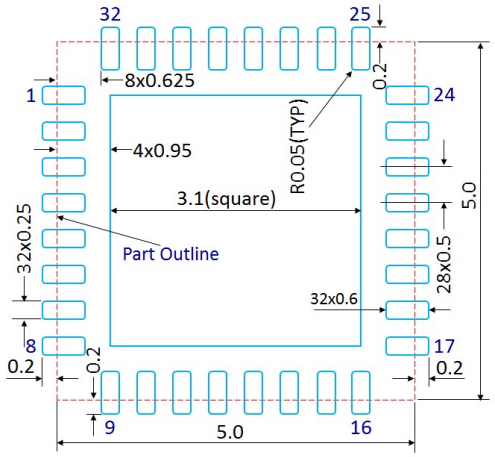
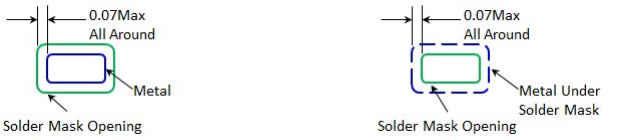


Figure 7 PCB Land Pattern
(Dimensions are in mm)



Non-Solder Mask Defined (Preferred)

Solder Mask Defined

Figure 8 Solder Mask Pattern
(Dimensions are in mm)

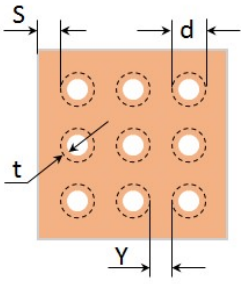


Figure 9 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

14.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125µm.

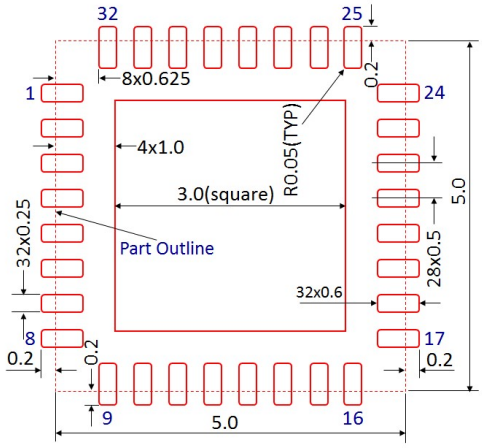


Figure 10 Stencil Openings
(Dimensions are in mm)

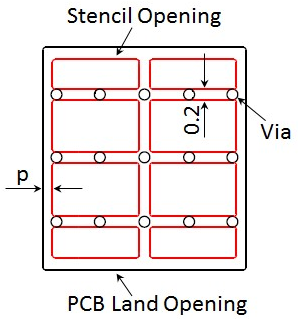


Figure 11 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

15.0 Tape and Reel Information

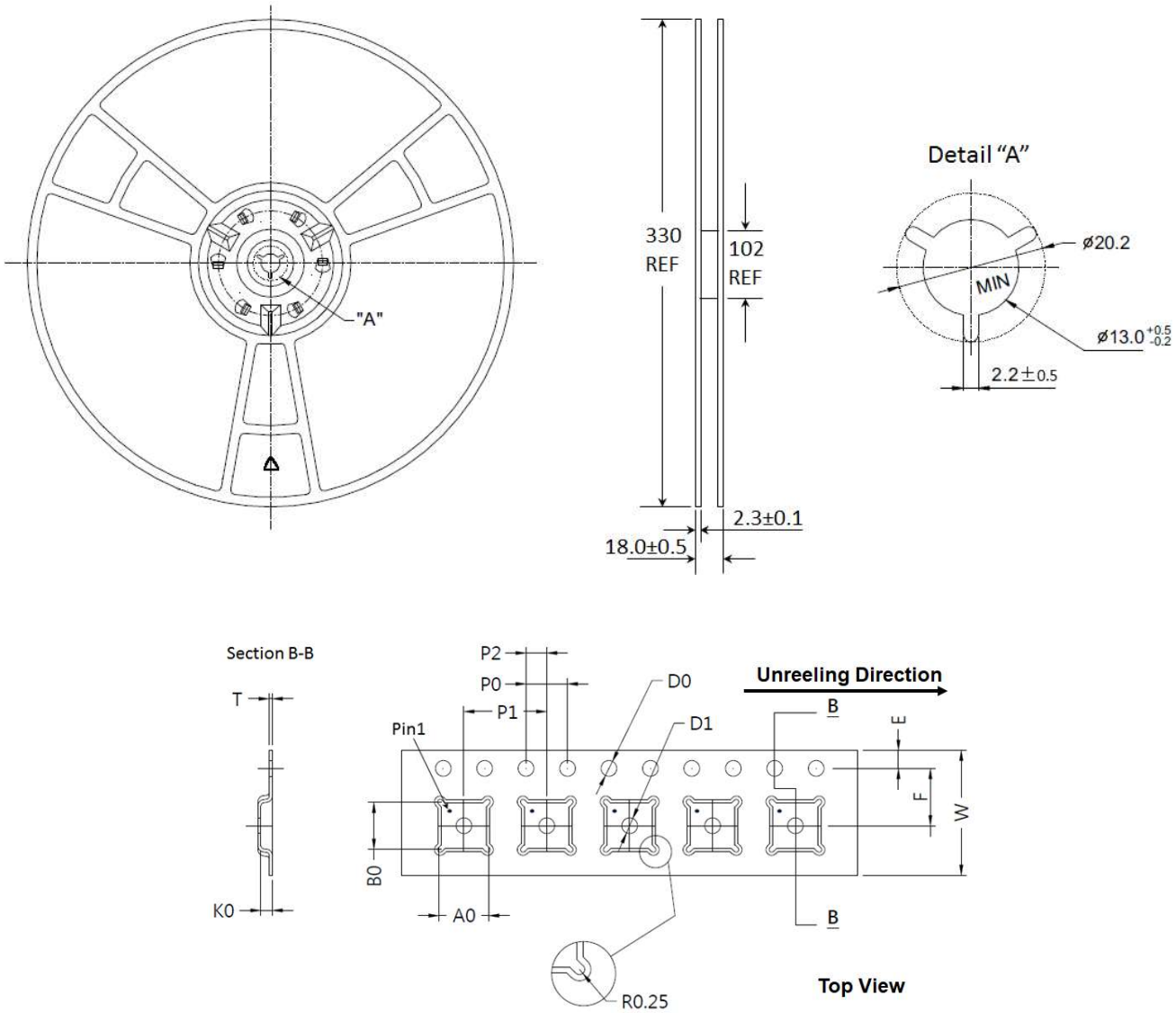


Figure 12 Tape and Reel Drawing

Table 8 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	5.35	±0.10	K0	1.10	±0.10
B0	5.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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