TS80210N - 50W CW, Broadband SPDT GaN RF Switch

1.0 Features

- Low insertion loss: 0.5dB @ 4GHz
- High isolation: 42dB @ 0.8GHz, 20dB @ 4GHz
- 50W CW, 125W Peak Power
- No external DC blocking capacitors on RF lines
- All RF ports OFF state
- Versatile 2.6-5.25V power supply
- Operating frequency: 30MHz to 4GHz

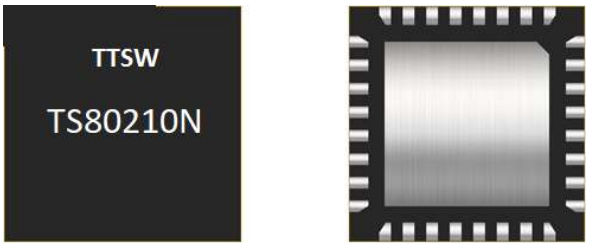


Figure 1 Device Image
(32 Pin 5×5×0.5mm QFN Package)

2.0 Applications

- Private mobile and military radios
- Public safety handsets
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Satellite terminals

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS80210N is a 2nd Generation symmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high power switching applications. With a simple broadband match, the TS80210N can cover 30M to 4GHz bandwidth and provide low insertion loss, high isolation, and high linearity within a small package size. TS80210N is an excellent switch for all applications requiring low insertion loss, high isolation, and high linearity within a small package size. This part has the internal charge pump disabled to eliminate the charge pump spurs. A -18V supply is needed on the VCP pin

The TS80210N is packaged into a compact Quad Flat No lead (QFN) 5x5mm 32 leads plastic package.

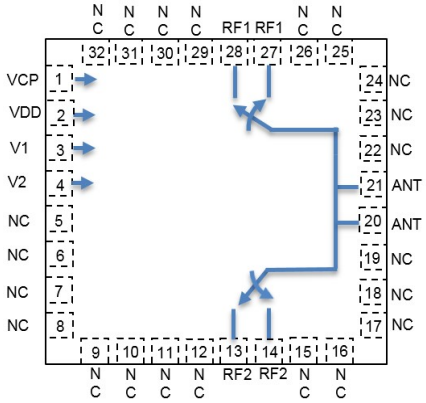


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1a Ordering Information

Device Part Number	Package Type	Eval Board Part Number
TS80210N	32 Pin 5×5×0.8mm QFN	TS80210N-EVB

Table 1b Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3,000	13” (330mm)	18mm

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	VCP	Negative Voltage Supply, -18V
2	VDD	DC power supply
3	V1	Switch control input 1
4	V2	Switch control input 2
5,6,7,8,9,10,11,16,17, 18,23,24,25,30,31,32	NC	No internal connection, can be grounded
12,15,19,22,26,29	NC	No internal connection. Do not connect to ground
13,14	RF2	RF port 2
20,21	ANT	Antenna port
27,28	RF1	RF port 1

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias, and adequate heat sinking must be used to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	5.5	V
Storage Temperature Range	T_{st}	-55 to +125	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+140	°C
Maximum RF input power(400MHz~4000MHz)	RFx/ANT	47	dBm
Maximum RF input power(30MHz~400MHz)	RFx/ANT	46	dBm
Thermal Ratings			

Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	7.0	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$	≤ 26	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:
Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+3.3V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency		30		4000	MHz
Insertion loss, RFx	800MHz		0.2	0.35	dB
	1.95GHz		0.3		
	4.0GHz		0.5		
Isolation ANT-RFx	800MHz	38	42		dB
	1.95GHz		32		
	4.0GHz		20		
Return loss ANT, RFx	800MHz		19		dB
	1.95GHz		16		
	4.0GHz		15		
Harmonic distortion					
H2	800MHz, Pin=45dBm		-86		dBc
H3	800MHz, Pin=45dBm		-89		dBc
IIP3	800MHz		71		dBm
P0.1dB[1]	800MHz, CW	47	50		dBm
P0.1dB[1]	30MHz, CW		46		dBm
Peak P0.1dB[1]	800MHz, 1% duty cycle, 1 mS period.		51		dBm
Switching time	50% ctrl to 10/90% of the RF value is settled. CP=1nF to ground on VCP pin.		5.2		μs
VCP	Iload of 10uA	-19	-18	-17	V
VCP Sourcing Current	Sourcing current of external VCP supply	100			uA
Control voltage	Power Supply VDD	2.6	3.3	5.25	V
	All control pins high, V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control current	All control pins low, I_{il}		0		μA
	All control pins high, I_{ih}			7.5	μA
Current consumption, IDD	Active mode (VDD on)		50	75	μA

Note:
[1] P0.1dB is a figure of merit.
[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	V2	Active RF Path
0	1	All OFF
0	0	ANT-RF1 ON
1	0	ANT-RF2 ON

Attention:
[1] **VDD should be applied first before VCP**. Minimum time between VDD and VCP should be 50usec.
[2] V1, or V2 can be toggled/switched after VCP has settled.

9.0 Evaluation Board (matched)

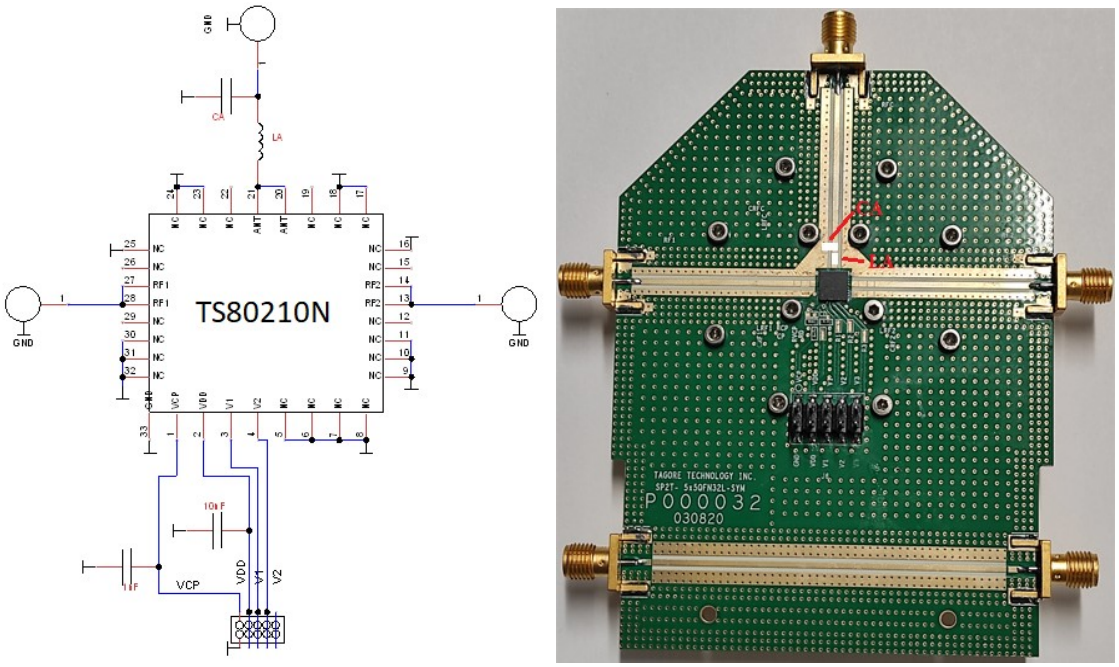


Figure 3 Evaluation Board and Schematic

Attention:
[1] 33 refers to the center pad of the device. Multiple Plugged through hole vias should be added on this Ground Pad and adequate heat sinking should be used.
[2] Place matching components close to pin of the part.

Table 6 Recommended Evaluation Board Component Values

Reference Designator	Value	Part #	Manufacturer
LA	0.8nH	0402DC-N80XJRU	Coilcraft
CA	0.5pF	0603	

10.0 Typical Characteristics

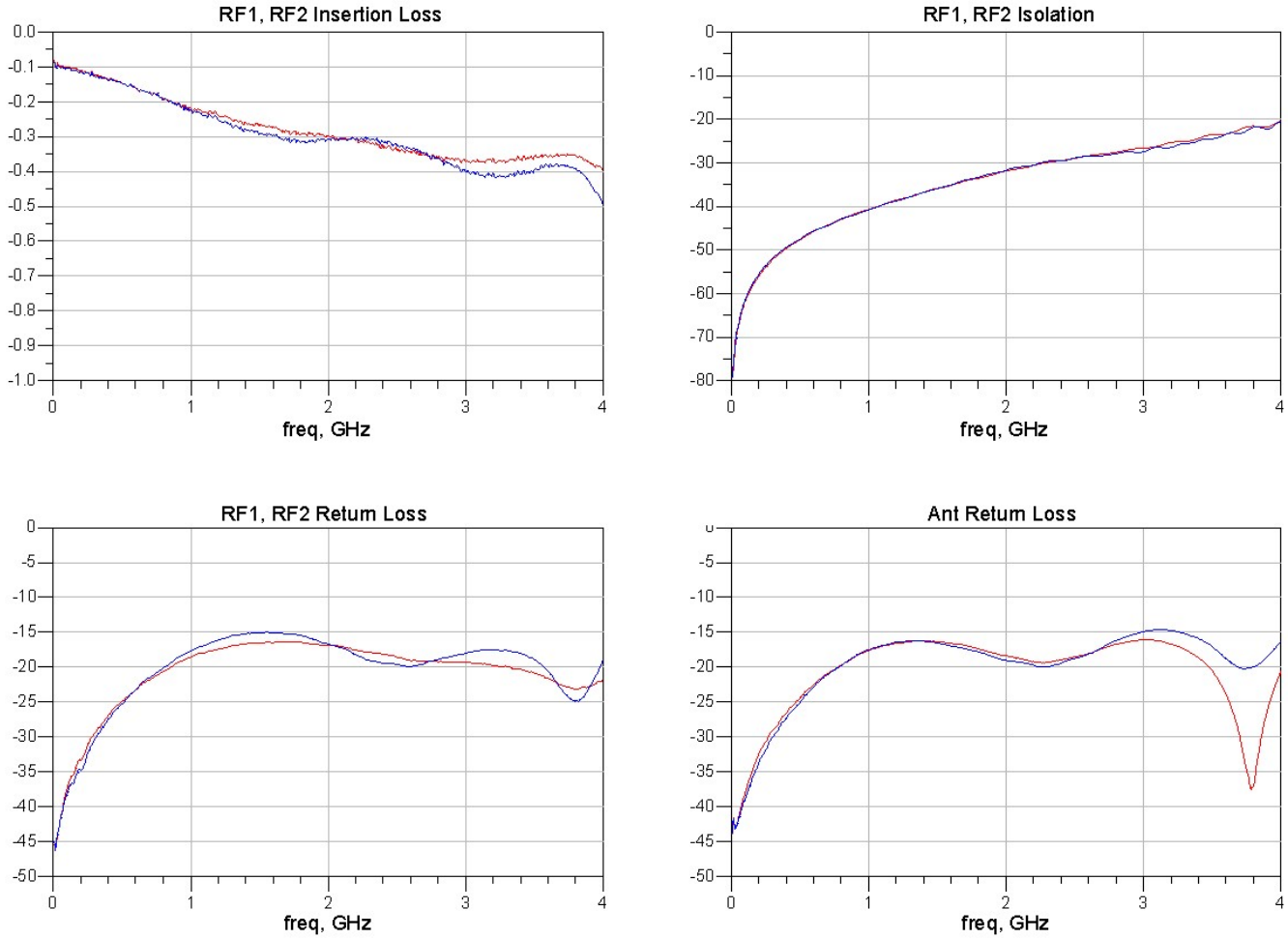


Figure 4 Evaluation Board Typical Characteristics (Matched)

11.0 Device Package Information

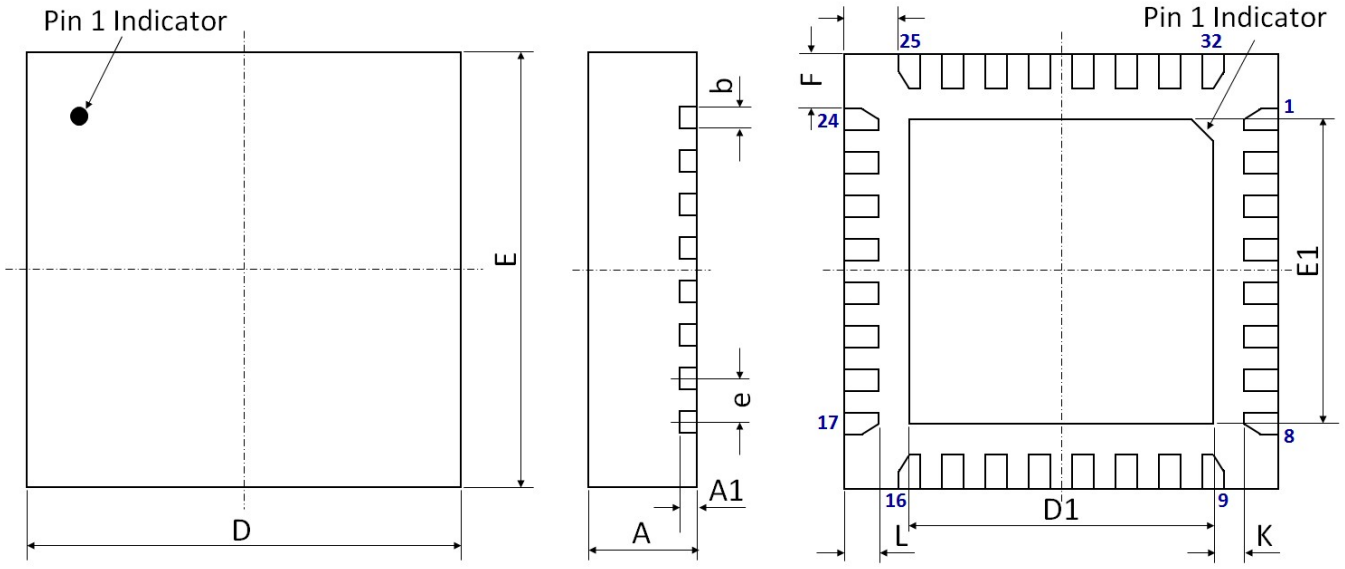


Figure 5 Device Package Drawing
(All dimensions are in mm)

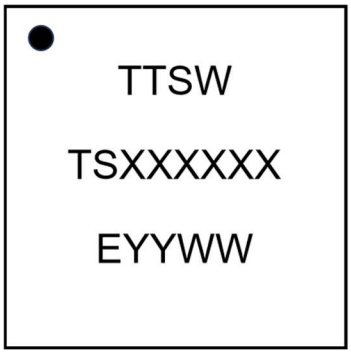
Table 7 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.8	±0.05	E	5.00 BSC	±0.05
A1	0.203	±0.02	E1	3.10	±0.06
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	5.00 BSC	±0.05	G	0.625	±0.05
D1	3.10	±0.06	L	0.40	±0.05
e	0.50 BSC	±0.05	K	0.50	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention:
Please refer to application notes *TN-001* and *TN-003* at http://www.tagoretech.com for PCB and soldering related guidelines.

Top-marking specification:



● = Pin 1 indicator
TTSW = Tagore Technology SWitch
TSXXXXXX = Part number (8 digits max)
E = A fixed letter before the date code
YY = Last two digits of assembly year
WW = Assembly work week

12.0 PCB Land Design

Guidelines:
[1] 4-layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 5(X)×5(Y)=25.

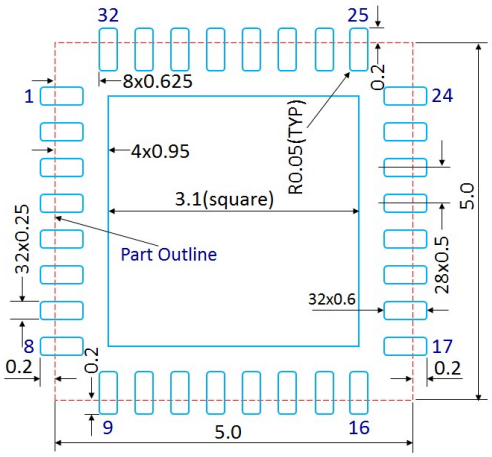
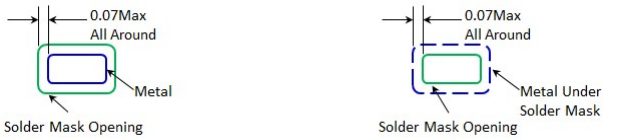


Figure 6 PCB Land Pattern
(Dimensions are in mm)



Non-Solder Mask Defined
(Preferred)

Solder Mask Defined

Figure 7 Solder Mask Pattern
(Dimensions are in mm)

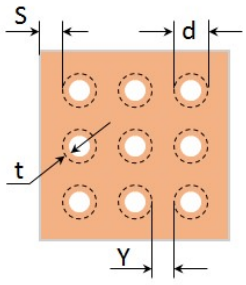


Figure 8 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

13.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125µm.

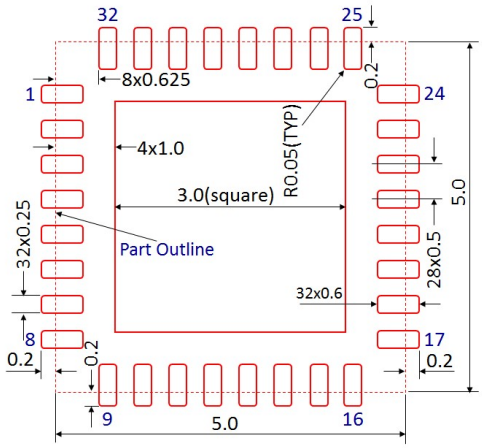


Figure 9 Stencil Openings
(Dimensions are in mm)

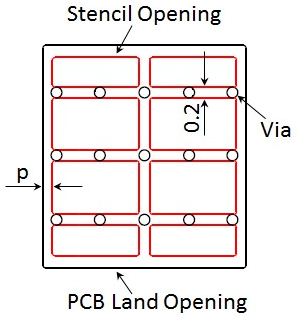


Figure 10 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

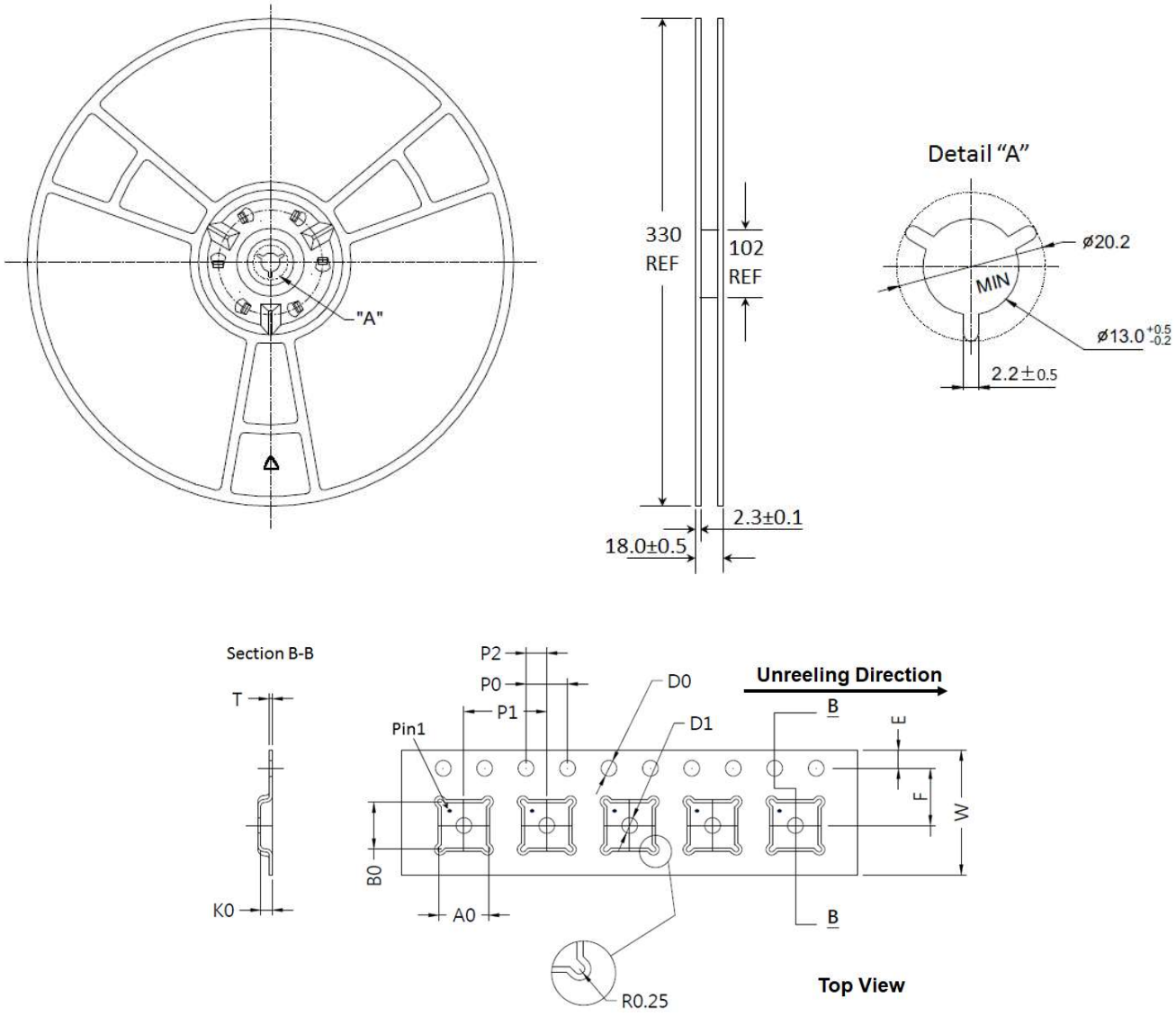


Figure 11 Tape and Reel Drawing

Table 8 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	5.35	±0.10	K0	1.10	±0.10
B0	5.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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