

TS8022L - 50W CW, Broadband SPDT GaN RF Switch

1.0 Features

- Low insertion loss: 0.5dB @ 4GHz
- High isolation: 42dB @ 0.8GHz, 20dB @ 4GHz
- 50W CW, 125W Peak Power
- No external DC blocking capacitors on RF lines
- All RF ports OFF state
- Versatile 2.6-5.25V power supply
- Operating frequency: 30MHz to 6GHz

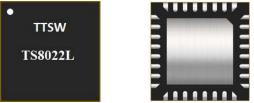


Figure 1 Device Image (32 Pin 4×4×0.8mm QFN Package)

2.0 Applications

- Private mobile and military radios
- Public safety handsets
- Cellular infrastructure
- Small cells
- LTE relays and micro-cells
- Satellite terminals

3.0 Description

The TS8022L is a 2nd Generation symmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high power switching applications. With a simple broadband match, the TS8022L can cover 30M to 6GHz bandwidth and provide low insertion loss, high isolation, and high linearity within a small package size. TS8022L is an excellent switch for all applications requiring low insertion loss, high isolation, and high linearity within a small package size.

The TS8022L is packaged into a compact Quad Flat No lead (QFN) 4x4mm 32 leads plastic package



RoHS/REACH/Halogen Free Compliance

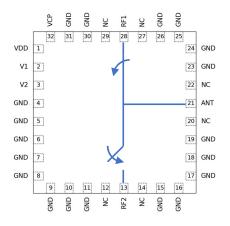


Figure 2 Function Block Diagram (Top View)

Note

 [1] Default state is ANT-RF1 when no control voltage is applied. See Section 8.0 for more details.
 [2] Pin 33 (not shown), is the pad/ground plane and must be soldered. Refer to schematic in Section 9.0.



4.0 Ordering Information

Table 1a Ordering Information

Device Part Number	Package Type	Eval Board Part Number
TS8022L	32 Pin 4×4×0.8mm QFN Package	TS8022L-EVB

Table 1b Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3,000	13" (330mm)	18mm

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	VDD	DC power supply
2	V1	Switch control input 1
3	V2	Switch control input 2
4,5,6,7,8,9,10,11,15,16,17, 18,19,23,24,25,26,30,31	NC	No connect, can be grounded
12,14,20,22,27,29	NC	No connect
13	RF2	RF port 2
21	ANT	Antenna port
28	RF1	RF port 1
32	VCP	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time.
33	GND	Ground thermal pad

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias, and adequate heat sinking must be used to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit		
Electrical Ratings					
Power Supply Voltage	VDD	5.5	V		
Storage Temperature Range	T _{st}	-55 to +125	°C		
Operating Temperature Range	T _{op}	-40 to +85	°C		
Maximum Junction Temperature	TJ	+140	°C		
Maximum RF input power(400MHz~4000MHz)	RFx/ANT	47	dBm		
Maximum RF input power(30MHz~400MHz)	RFx/ANT	46	dBm		



Thermal Ra	itings				
Thermal Resistance (junction-to-case) – Bottom side	Rejc	7.0	°C/W		
Thermal Resistance (junction-to-top)	Rejt	≤ 37	°C/W		
Soldering Temperature	T _{SOLD}	260	°C		
ESD Rati	ngs				
Human Body Model (HBM)	Level 1B	500 to <1000	V		
Charged Device Model (CDM)	Level C3	≥1000	V		
Moisture Rating					
Moisture Sensitivity Level	MSL	1	-		

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.



7.0 Electrical Specifications

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency		30		6000	MHz
	800MHz		0.2	0.35	
Insertion loss, RFx	1.95GHz		0.3		dB
Insenion loss, RFX	4.0GHz		0.5		UD
	6.0GHz (matched)		0.65		
	800MHz	38	42		
Isolation ANT-RFx	1.95GHz		32		
	4.0GHz		20		dB
	6.0GHz (matched)		19		
	800MHz		19		
Return loss ANT,	1.95GHz		16		
Return loss ANT, RFx	4.0GHz		15		dB
	6.0GHz (matched)		17		
Harmonic distortion					
H2	800MHz, Pin=45dBm		-86		dBc
H3	800MHz, Pin=45dBm		-89		dBc
IIP3	800MHz		71		dBm
P0.1dB ^[1]	800MHz, CW	47	50		dBm
P0.1dB ^[1]	30MHz, CW		46		dBm
Peak P0.1dB ^[1]	800MHz, 1% duty cycle, 1 mS period.		51		dBm
Switching time	50% ctrl to 10/90% of the RF value is settled. CP=1nF to ground on VCP pin.		5.2		μs
	Power Supply VDD	2.6	3.3	5.25	V
Control voltage	All control pins high, V _{ih}	1.0	3.3	5.25	V
een er renage	All control pins low, Vii	-0.3		0.5	V
O an track as small at	All control pins low, Iii		0		μA
Control current	All control pins high, I _{ih}			7.5	μA
Current consumption, IDD	Active mode (VDD on)		160	200	μΑ

Note:

[1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.



8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	V2	Active RF Path
0	1	All OFF
0	0	ANT-RF1 ON
1	0	ANT-RF2 ON

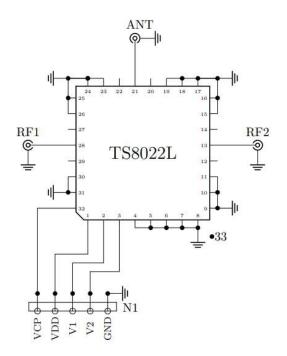
Attention:

[1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.

[2] There are internal pull-downs to ground on both V1 and V2 control pins, the state at start-up without any control voltage applied will be ANT-RF1 ON.

[3] If all OFF state is not used, the switch can be operated with single control pin V1.

9.0 Evaluation Board and Schematic



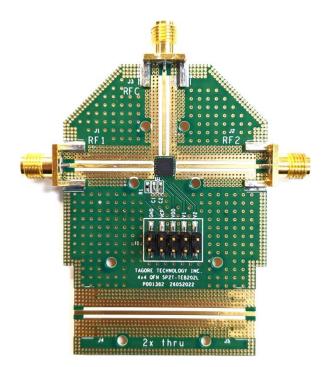


Figure 3 Evaluation Board and Schematic

Attention:

[1] 33 refers to the center pad of the device. Multiple Plugged through hole vias should be added on this Ground Pad and adequate heat sinking should be used.

[2] The purpose of connection between VCP and connector N1 is to monitor VCP, do not apply external voltage to VCP.

[3] Place matching components close to pin of the part.



10.1 Typical Characteristics (unmatched)

TS8022L

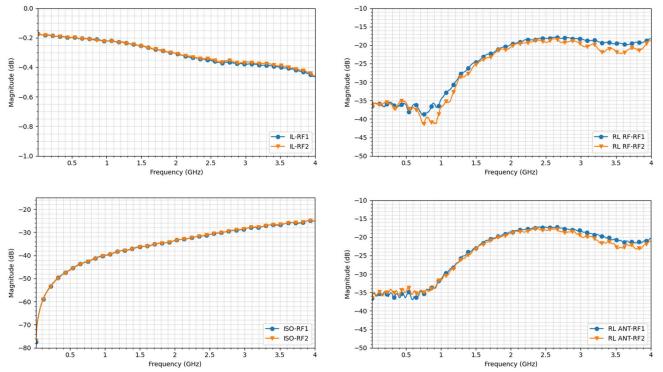


Figure 4.1 Typical Characteristics (unmatched)



TS8022L

10.2 Typical Characteristics (1000 MHz - 6000 MHz)

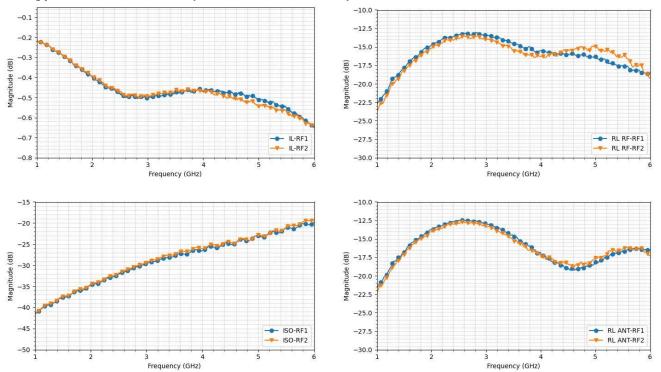


Figure 4.2 Typical Characteristics (1000 MHz - 6000 MHz)



11.1 Bill of Materials – (Unmatched)

Table 6.1 Bill of Materials – Unmatched

Componer	nt Part Number	Description	Notes
CP	GRM155R61E104KA87D	Ceramic capacitor, 0.1 µF, 25 V, ±10%.	
CD	GRM155R71H103KA88	Ceramic capacitor, 10 nF, 50 V, ±15%.	

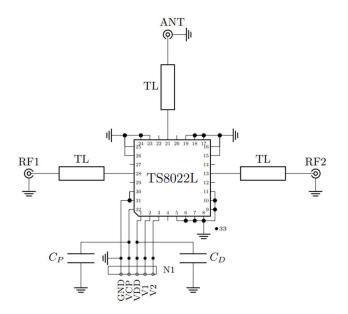


Figure 5.1 Schematic for Unmatched Condition



11.2 Bill of Materials - (1000MHz - 6000MHz)

Tuble			
Ref	Part Number/Value	Description	Notes
CP	GRM155R61E104KA87D	Ceramic capacitor, 0.1 µF, 25 V, ±10%.	
CD	GRM155R71H103KA88	Ceramic capacitor, 10 nF, 50 V, ±15%.	
T _{0a}	2.2mm	PCB transmission line length.	
T _{1a}	0.3mm	PCB transmission line length.	Used to solder capacitors at switch reference plane.
T _{2a}	0.3mm	PCB transmission line length.	Used to solder capacitors at switch reference plane.
C _{0a}	600S0R3BT250XT	Ceramic capacitor, 0.3 pF, 250V, ± 0.1pF.	
C _{1a}	0603N0R1BW251	Ceramic capacitor, 0.1 pF, 250V, ± 0.1pF.	
C _{2a}	0603N0R1BW251	Ceramic capacitor, 0.1 pF, 250V, ± 0.1pF.	

Table 6.2 Bill of Materials - (1000MHz - 6000MHz)

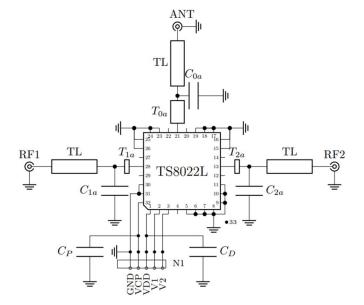


Figure 5.2 Schematic for Matching (1000 MHz – 6000MHz)



12.0 Device Package Information

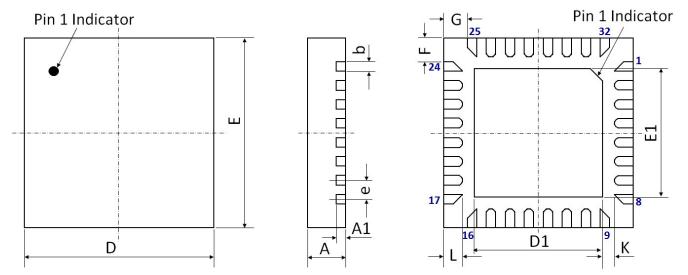


Figure 6 Device Package Drawing (All dimensions are in mm)

Table 7 Device Package Dimensions

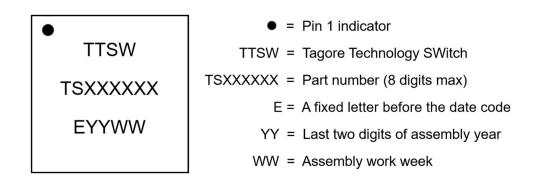
Dimension (mm)	Value (mm)	Tolerance (mm)	Dimension (mm)	Value (mm)	Tolerance (mm)
A	0.80	±0.05	E	4.00 BSC	±0.05
A1	0.203	±0.02	E1	2.70	±0.05
b	0.20	+0.05/-0.07	F	0.50	±0.05
D	4.00 BSC	±0.05	G	0.50	±0.05
D1	2.70	±0.05	L	0.40	±0.05
е	0.40 BSC	±0.05	K	0.25	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5µm ~ 20µm (Typical 10µm ~ 12µm)

Attention:

Please refer to application notes *TN-001* and *TN-003* at http://www.tagoretech.com for PCB and soldering related guidelines.

Top-marking specification:





13.0 PCB Land Design

Guidelines:

[1] 4-layer PCB is recommended.

- [2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
- [3] Thermal vias shall only be placed on the center pad.
- [4] The maximum via number for the center pad is $4(X) \times 4(Y) = 16$.

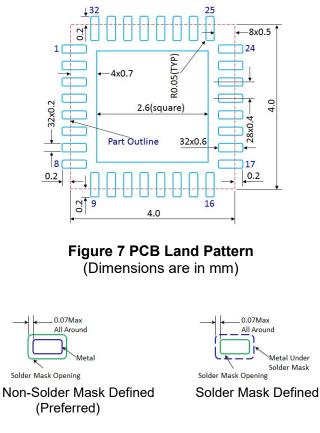


Figure 8 Solder Mask Pattern

(Dimensions are in mm)

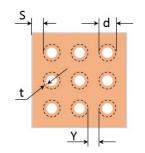


Figure 9 Thermal Via Pattern (Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25µm or 50µm)



14.0 PCB Stencil Design

Guidelines:

- [1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- [2] Stencil thickness is recommended to be 125µm.

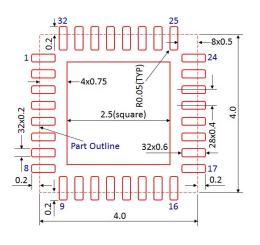


Figure 10 Stencil Openings (Dimensions are in mm)

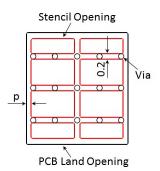
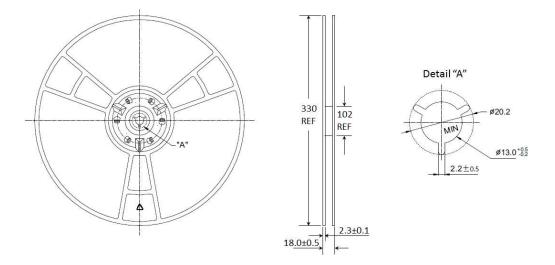


Figure 11 Stencil Openings Shall not Cover Via Areas If Possible (Dimensions are in mm)



15.0 Tape and Reel Information



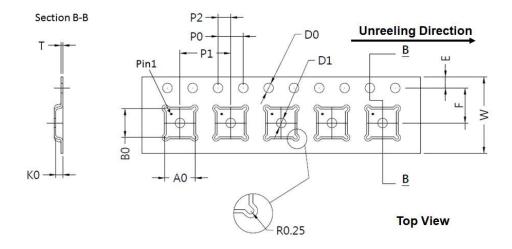


Figure 12 Tape and Reel Drawing

Table 8 Tape and Reel Dimensions

Dimension (mm)	Value (mm)	Tolerance (mm)	Dimension (mm)	Value (mm)	Tolerance (mm)
A0	5.35	±0.10	K0	1.10	±0.10
B0	5.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	Т	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30



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