

TS8242FK - 10W CW, Broadband SP4T GaN RF Switch

1.0 Features

- Low insertion loss: 0.2 @ 800MHz
- Low insertion loss: 0.3 @ 2700MHz
- High isolation: 40 @ 800MHz
- High isolation: 25 @ 2700MHz
- 40dBm CW, 45dBm Peak Power
- No external DC blocking capacitors on RF lines
- Versatile 2.6-5.25V power supply
- Operating frequency: 30 MHz to 5.0 GHz

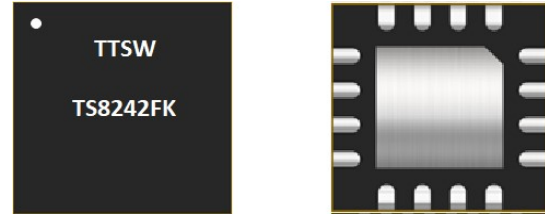


Figure 1 Device Image
(16 Pin 3x3x0.8mm QFN Package)

2.0 Applications

- Private mobile radio handsets
- Public safety handsets
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Satellite terminals



RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS8242FK is a symmetrical reflective Single Pole Four Throws (SP4T) switch designed for broadband, high power switching applications. Its broadband behavior from 30 MHz to 5.0 GHz frequencies makes the TS8242FK an excellent switch for all applications requiring low insertion loss, high isolation, and high linearity within a small package size.

The TS8242FK is packaged into a compact Quad Flat No lead (QFN) 3x3mm 16 leads plastic package.

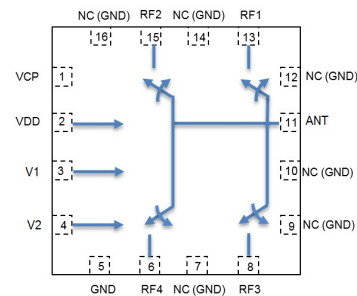


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1a Ordering Information

| Device Part Number | Package Type | Eval Board Part Number |
|--------------------|----------------------|------------------------|
| TS8242FK | 16 Pin 3×3×0.8mm QFN | TS8242FK-EVB |

Table 1b Tape and Reel Information

| Form | Quantity | Reel Diameter | Reel Width |
|---------------|----------|---------------|------------|
| Tape and Reel | 3,000 | 13" (330mm) | 18mm |

5.0 Pin Description

Table 2 Pin Definition

| Pin Number | Pin Name | Description |
|-------------------|----------|--|
| 1 | VCP | Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time. |
| 2 | VDD | DC power supply |
| 3 | V1 | Switch control input 1 |
| 4 | V2 | Switch control input 2 |
| 6 | RF4 | RF port 4 |
| 5,7,9,10,12,14,16 | NC | No internal connection, can be grounded |
| 8 | RF3 | RF port 3 |
| 11 | ANT | Antenna port |
| 13 | RF1 | RF port 1 |
| 15 | RF2 | RF port 2 |

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @ $T_A=+25^{\circ}\text{C}$ Unless Otherwise Specified

| Parameter | Symbol | Value | Unit |
|---|-----------------|--------------|----------------------|
| Electrical Ratings | | | |
| Power Supply Voltage | VDD | 5.5 | V |
| Storage Temperature Range | T_{st} | -55 to +125 | $^{\circ}\text{C}$ |
| Operating Temperature Range | T_{op} | -40 to +85 | $^{\circ}\text{C}$ |
| Maximum Junction Temperature | T_J | +140 | $^{\circ}\text{C}$ |
| Maximum RF input power | RFx/ANT | 40 | dBm |
| Thermal Ratings | | | |
| Thermal Resistance (junction-to-case) – Bottom side | $R_{\theta JC}$ | 30 | $^{\circ}\text{C/W}$ |
| Thermal Resistance (junction-to-top) | $R_{\theta JT}$ | 39 | $^{\circ}\text{C/W}$ |
| Soldering Temperature | T_{SOLD} | 260 | $^{\circ}\text{C}$ |
| ESD Ratings | | | |
| Human Body Model (HBM) | Level 1B | 500 to <1000 | V |

| | | | |
|----------------------------|----------|-------|---|
| Charged Device Model (CDM) | Level C3 | ≥1000 | V |
| Moisture Rating | | | |
| Moisture Sensitivity Level | MSL | 1 | - |

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @ $T_A=+25^{\circ}\text{C}$ Unless Otherwise Specified; $V_{DD}=+2.7\text{V}$; 50Ω Source/Load.

| Parameter | Condition | Minimum | Typical | Maximum | Unit |
|-------------------------------|---|---------|---------|---------|---------------|
| Operating Frequency | | 30 | | 5000 | MHz |
| Insertion Loss, RFX | 400MHz | | 0.2 | | dB |
| | 800MHz | | 0.25 | 0.40 | |
| | 1.95GHz | | 0.3 | | |
| | 4.0GHz(matched) | | 0.5 | | |
| Isolation ANT-RFX | 400MHz | | 45 | | dB |
| | 800MHz | 36 | 40 | | |
| | 1.95GHz | | 30 | | |
| | 4.0GHz(matched) | | 20 | | |
| Return Loss ANT-RFX | 400MHz | | 28 | | dB |
| | 800MHz | | 24 | | |
| | 1.95GHz | | 24 | | |
| | 4.0GHz(matched) | | 18 | | |
| H2 | 800MHz, CW, Pin=40dBm | | 86 | | dBc |
| H3 | 800MHz, CW, Pin=40dBm | | 89 | | dBc |
| IIP3 | 800MHz | | 74 | | dBm |
| CW P0.1dB ^[1] | 800MHz | 40 | 43 | | dBm |
| Peak P0.1dB ^[1] | 800MHz, Duty cycle 1%, Period 1 mS | 45 | 48 | | dBm |
| Switching Time | 50% ctrl to 10/90% of the RF value is settled. C1=1nF (refer to Figure 3) | | 0.6 | | μs |
| Control Voltage | Power supply VDD | 2.6 | 3.3 | 5.25 | V |
| | All control pins high, V_{ih} | 1.0 | 3.3 | 5.25 | V |
| | All control pins low, V_{il} | -0.3 | | 0.5 | V |
| Control Current | All control pins low, I_{il} | | 0 | | μA |
| | All control pins high, I_{ih} | | | 7.5 | μA |
| Current Consumption, I_{DD} | Active mode | | 170 | 210 | μA |

Note:

[1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

| V1 | V2 | Active RF Path |
|----|----|----------------|
| 0 | 0 | ANT-RF1 |
| 1 | 0 | ANT-RF2 |
| 0 | 1 | ANT-RF3 |
| 1 | 1 | ANT-RF4 |

Attention:

- [1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.
- [2] There are internal pull-downs to ground on both V1 and V2 control pins, the state at start-up without any control voltage applied will be ANT-RF1 ON.

9.0 Evaluation Board (no match)

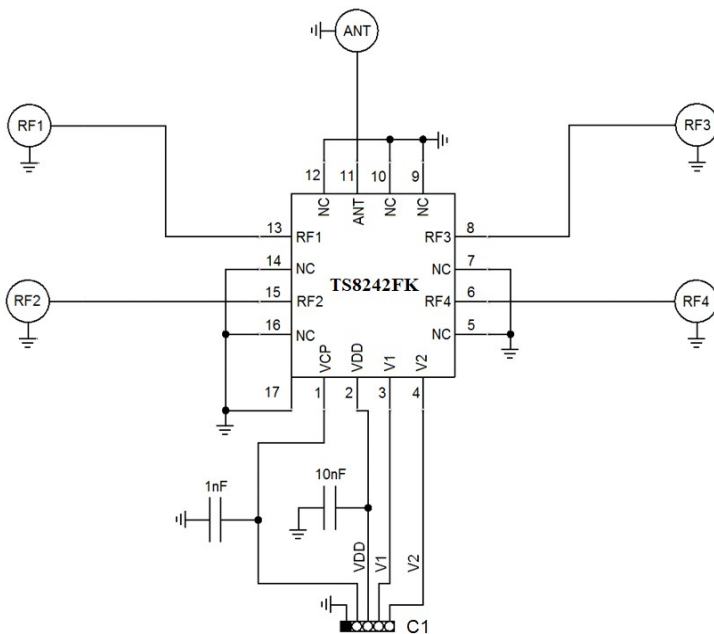


Figure 3 Evaluation Board Schematic

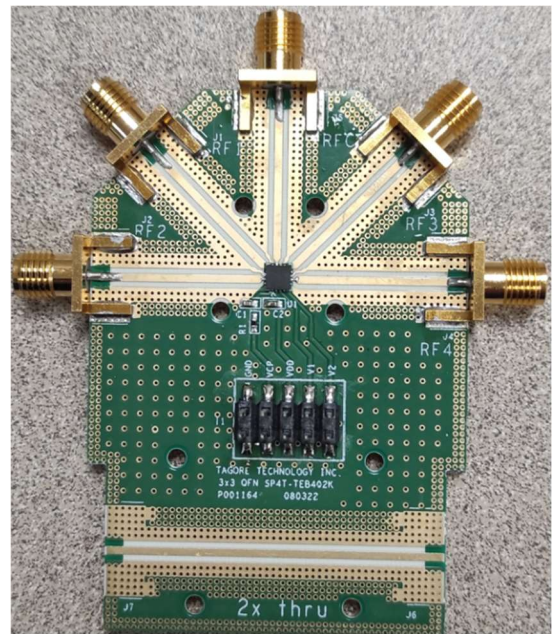


Figure 4 Evaluation Board Image

Attention:

- [1] 17 refers to the center pad of the device.
- [2] The purpose of connection between VCP and connector C1 is to monitor VCP, do not apply external voltage to VCP.
- [3] matched EVB has a series 1nH inductor, and then a shunt 0.3pF capacitor at TS8242FK Ant port.

10.0 Typical Characteristics(matched)

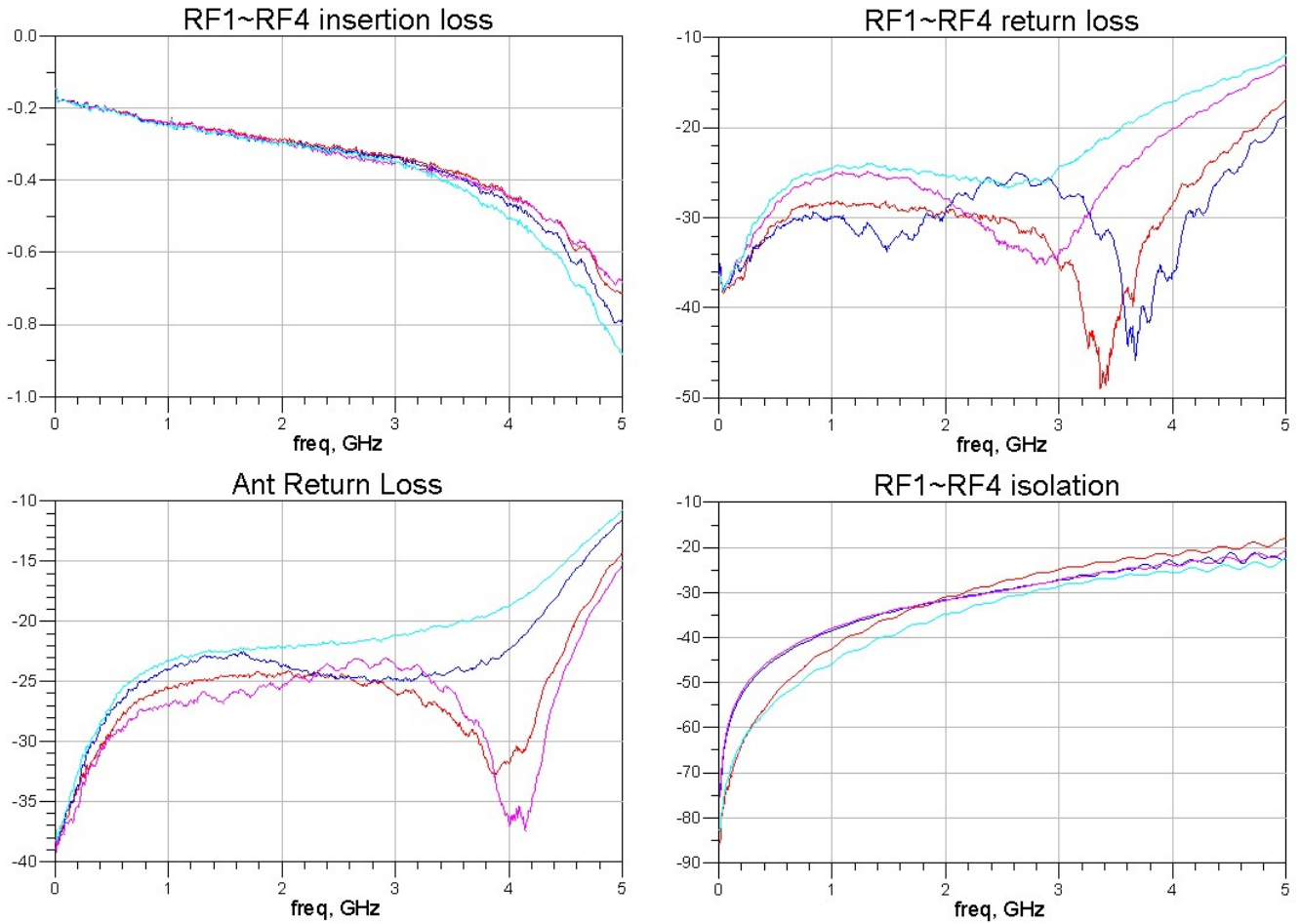


Figure 5 Typical Characteristics of TS8242FK

11.0 Device Package Information

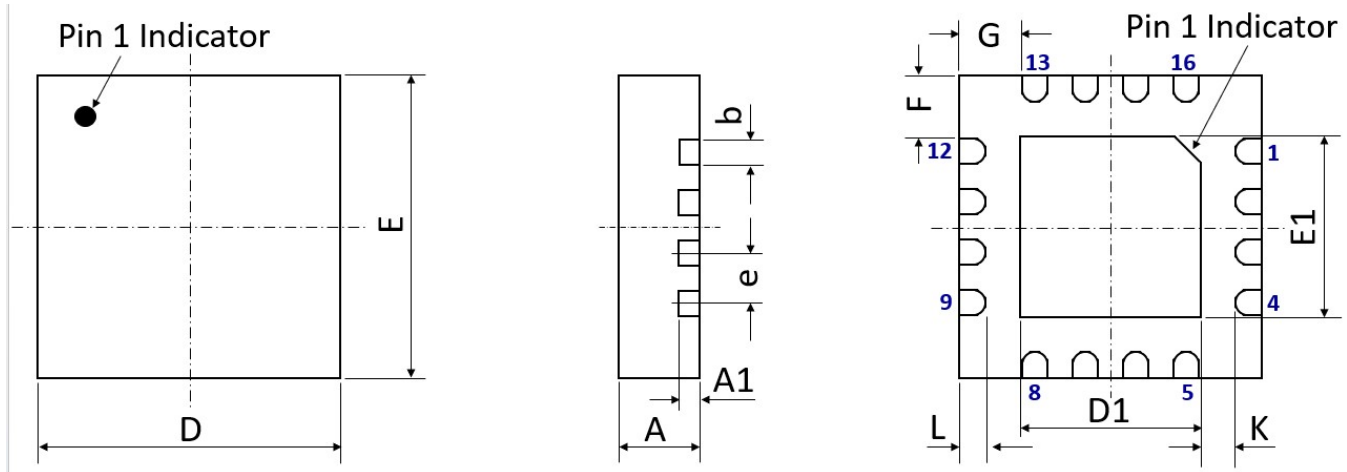


Figure 6 Device Package Drawing
(All dimensions are in mm)

Table 6 Device Package Dimensions

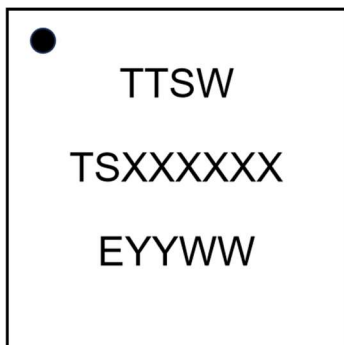
| Dimension (mm) | Value (mm) | Tolerance (mm) | Dimension (mm) | Value (mm) | Tolerance (mm) |
|----------------|------------|----------------|----------------|------------|----------------|
| A | 0.80 | ±0.05 | E | 3.00 BSC | ±0.05 |
| A1 | 0.203 | ±0.02 | E1 | 1.70 | ±0.05 |
| b | 0.25 | ±0.05 | F | 0.625 | ±0.05 |
| D | 3.00 BSC | ±0.05 | G | 0.625 | ±0.05 |
| D1 | 1.70 | ±0.05 | L | 0.25 | ±0.05 |
| e | 0.50 BSC | ±0.05 | K | 0.40 | ±0.05 |

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5µm ~ 20µm (Typical 10µm ~ 12µm)

Attention:

Please refer to application notes [TN-001](#) and [TN-002](#) at <http://www.tagoretech.com> for PCB and soldering related guidelines.

Top-marking specification:



- = Pin 1 indicator
- TTSW = Tagore Technology SWITCH
- TSXXXXXX = Part number (8 digits max)
- E = A fixed letter before the date code
- YY = Last two digits of assembly year
- WW = Assembly work week

12.0 PCB Land Design

Guidelines:

- [1] 4-layer PCB is recommended.
- [2] Via diameter is recommended to be 0.3mm to prevent solder wicking inside the vias.
- [3] Thermal vias shall only be placed on the center pad.
- [4] The maximum via number for the center pad is $3(X) \times 3(Y) = 9$.

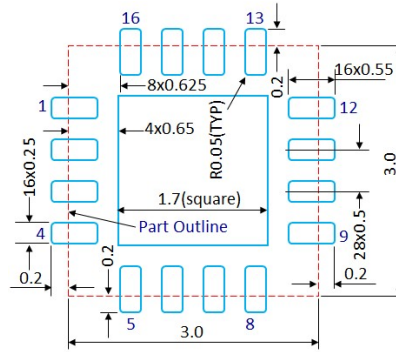


Figure 7 PCB Land Pattern
(Dimensions are in mm)

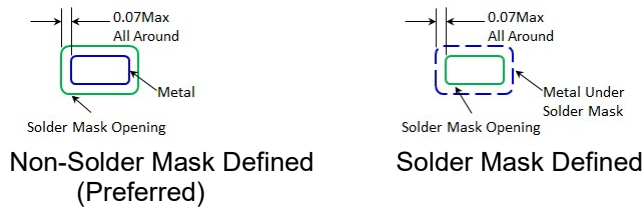


Figure 8 Solder Mask Pattern
(Dimensions are in mm)

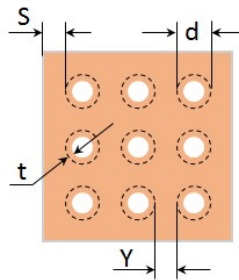


Figure 9 Thermal Via Pattern

(Recommended Values: $S \geq 0.15\text{mm}$; $Y \geq 0.20\text{mm}$; $d = 0.3\text{mm}$; Plating Thickness $t = 25\mu\text{m}$ or $50\mu\text{m}$)

13.0 PCB Stencil Design

Guidelines:

- [1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- [2] Stencil thickness is recommended to be 125µm.

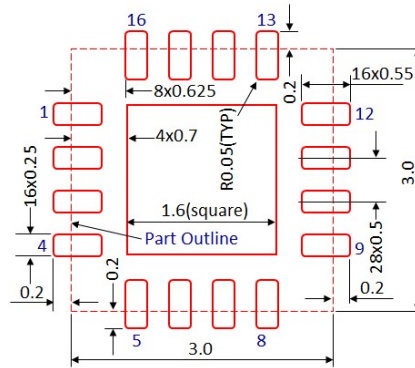


Figure 10 Stencil Openings
(Dimensions are in mm)

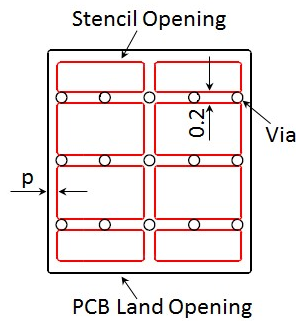


Figure 11 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

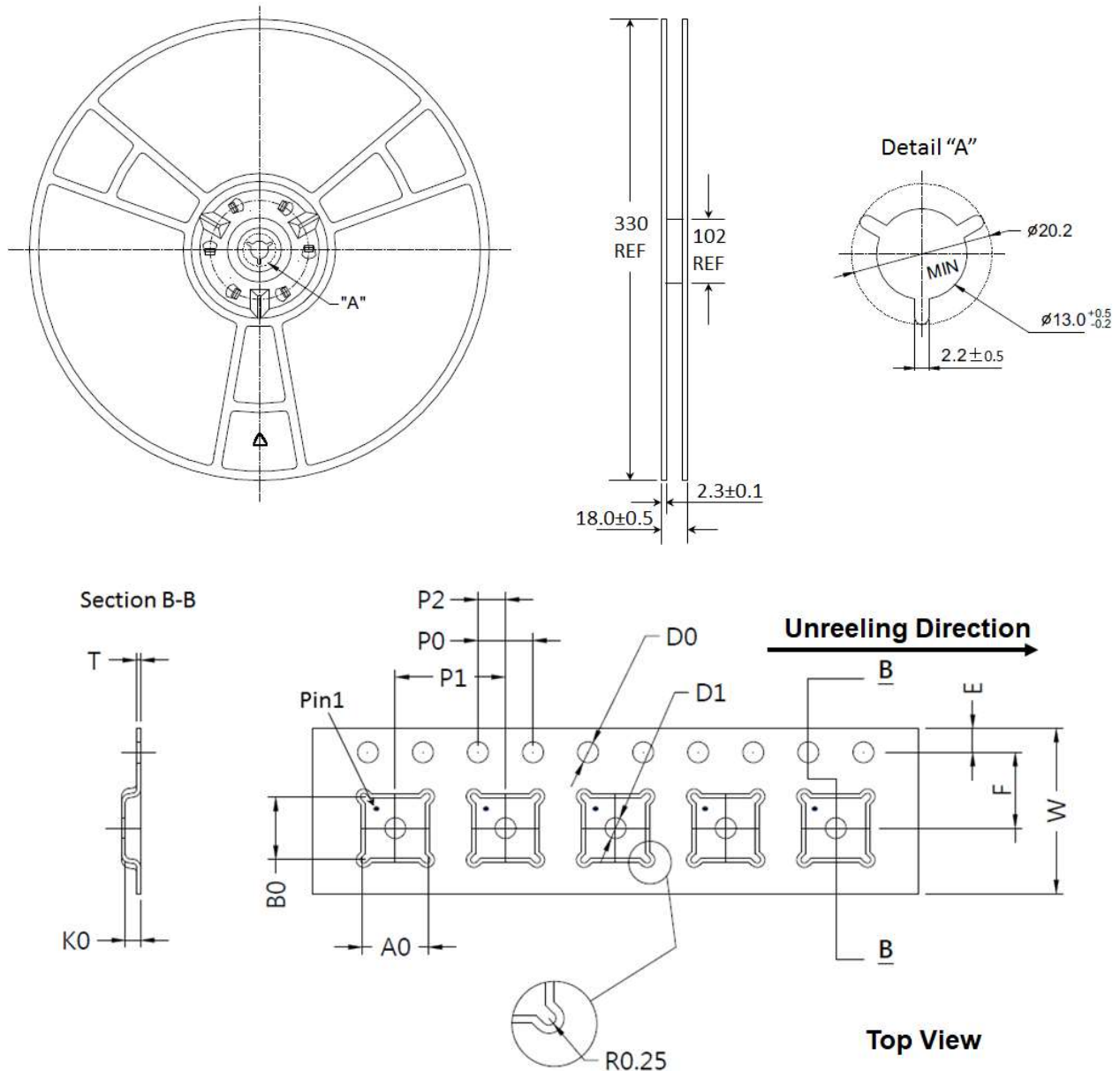


Figure 12 Tape and Reel Drawing

Table 7 Tape and Reel Dimensions

| Dimension (mm) | Value (mm) | Tolerance (mm) | Dimension (mm) | Value (mm) | Tolerance (mm) |
|----------------|------------|----------------|----------------|------------|----------------|
| A0 | 3.35 | ±0.10 | K0 | 1.10 | ±0.10 |
| B0 | 3.35 | ±0.10 | P0 | 4.00 | ±0.10 |
| D0 | 1.50 | +0.10/-0.00 | P1 | 8.00 | ±0.10 |
| D1 | 1.50 | +0.10/-0.00 | P2 | 2.00 | ±0.05 |
| E | 1.75 | ±0.10 | T | 0.30 | ±0.05 |
| F | 5.50 | ±0.05 | W | 12.00 | ±0.30 |

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