SP8T 15 W Power Switch 1 MHz to 4.0 GHz

Features

- Single pole eight throw (SP8T)
- Frequency Range 1 MHz to 4.0 GHz
- Low insertion loss:
  0.46 dB @ 1.0 GHz
  0.81 dB @ 3.0 GHz
- Isolation:
  32 dB @ 1.0 GHz, 22 dB @ 3.0 GHz
- 15 W power switch
- $P_{0.1dB}$ = 42 dBm @ 800 MHz
- Switching time 0.5 µs
- Flip bit V_5 for filter and delay line banks
- Low power consumption, less than 1 mW
- Versatile 2.6 V – 5.25 V power supply
- No need to supply negative voltages

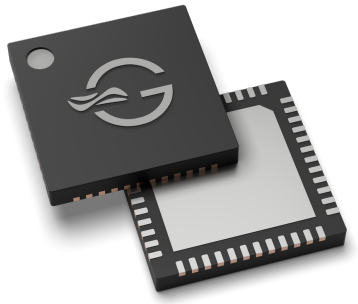


Figure 1: TS8381M in 6.0 x 6.0 mm^2 QFN 48-pin package.

Applications

- Filter banks, delay line banks and band switching
- Private mobile and defense radios
- Public safety handsets
- Cellular infrastructure
- Satellite terminals
- Datalinks

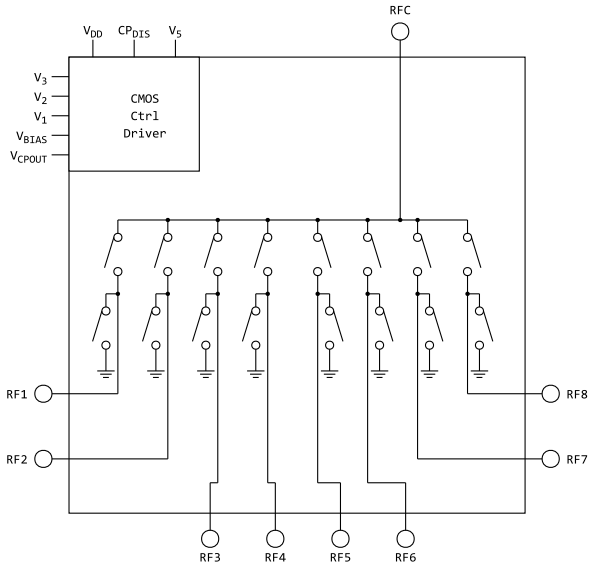


Figure 2: TS8381M functional diagram

General Description

The TS8381M is a 15 W reflective Single Pole Eight Throw (SP8T) switch based on GaN technology, designed for band and filter bank switching in high power radios. The TS8381M covers 1 MHz to 4.0 GHz and provides low insertion loss and high linearity: without matching up to 3.0 GHz, with a simple matching on the antenna port up to 4.0 GHz. Each throw has a series and a shunt switch. The TS8381M operates from a single standard V_{DD} supply; no external negative voltages are required, as the bias is generated with an internal charge pump.

The TS8381M is housed in a compact 6.0×6.0 mm^2 48-lead Quad Flat No-lead (QFN) plastic package.

RoHS

RoHS/REACH/Halogen free

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Ordering information

Table 1: Ordering Information

Device Part Number	Package Type	Notes
TS8381M	48 Pin 6.0x6.0x0.85 mm^3 QFN	Core part number
TS8381M-EVB	Evaluation Board	
TS8381MMTRPBF[1]	330 mm reel, 3 000 pcs	Full reel

[1] MTRPBF - M: Manufacturing, TR: Tape and Reel, and PBF: lead free.

Table 2: Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3 000	13” (330mm)	tbd

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Pin Assignment

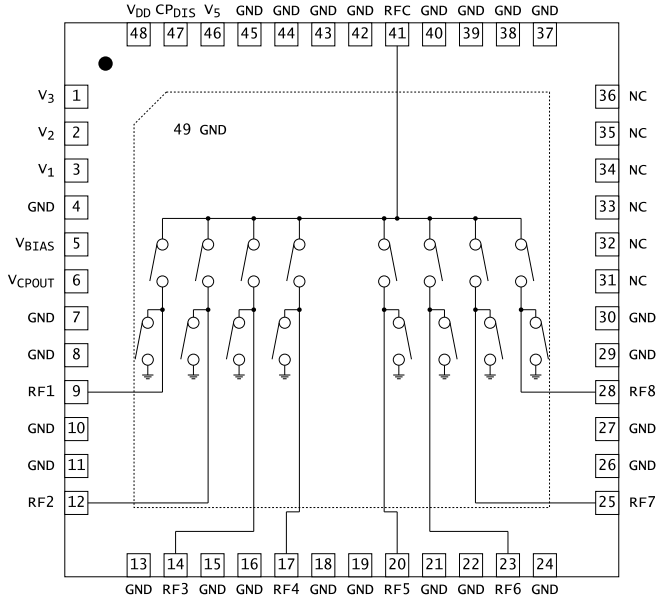


Figure 3: TS8381M pin assignment [top view]

Table 3: Pin Definition

Pin Number	Pin Name	Description
41	RFC (ANT)	RF common port (antenna port)
9	RF1	RF port 1
12	RF2	RF port 2
14	RF3	RF port 3
17	RF4	RF port 4
20	RF5	RF port 5
23	RF6	RF port 6
25	RF7	RF port 7
28	RF8	RF port 8
48	V_{DD}	DC Power Supply
47	CP_{DIS}	Disable Internal Charge Pump[3]
5	V_{BIAS}	Bias voltage input, -18 V...-20 V, either from external source or internal charge pump
6	V_{CPOUT}	Internal charge pump voltage output
3	V_1	Switch control input 1
2	V_2	Switch control input 2
1	V_3	Switch control input 3
46	V_5	Switch control input 5, flip bit[4]
4	GND	Ground of the control circuitry
7,8,10,11,13,15,16,18,19,21,22 24,26,27,29,30,37,38,39,40 42,43,44,45	GND	Connect to ground[2]
31,32,33,34,35,36	NC	Not connected, connect to ground[2]
49 [1]	GND	Ground thermal pad, please connect to GND

[1] The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias, and adequate heat sinking must be used to ensure proper operation and thermal management.
[2] These pins are NC pins inside the package. To avoid floating pins around RF lines, we request these to be connected to ground.
[3] Feeding V_{DD} to this pin disables the internal charge pump. In this case, ground V_{CPOUT} and feed -18 V...-20 V to V_{BIAS}.
[4] Flip bit: with V_5 high, the control word of RFx selects $RF(9-x)$, see Switch Control Table.

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Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings $T_A = +25$°C unless otherwise specified[1].

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	V_{DD}	5.5	V
Maximum (min) bias voltage	V_{BIAS}	-21	V
Storage Temperature Range	T_{st}	−55 – 125	°C
Operating Temperature Range	T_{op}	−40 – 85	°C
Maximum Junction Temperature	T_j	+140	°C
Maximum RF CW input power	RFx / RFC	tbd	dBm
Maximum RF peak input power, 1% duty cycle, 10μs pulse	RFx / RFC	tbd	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta jc}$	tbd	°C/W
Soldering Temperature	T_{solder}	+260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 – $<$1000	V
Charged Device Model (CDM)	Level C3	$\geq$1000	V
Moisture Rating			
Moisture Sensitivity Level[2]	MSL	1	

[1] Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and can cause permanent damage to the device. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit. Functional operation of the device is not implied in any conditions above those indicated in the Electrical Specifications section.

[2] Tagore recommends to store parts in moisture barrier bags to preserve solderability.

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Electrical Specifications

Table 5: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	1		4000	MHz
Insertion loss[1]	30 MHz		0.34		dB
unmatched, up to 3.0 GHz	1.0 GHz		0.46		dB
RFC – RFx	2.0 GHz		0.58		dB
	3.0 GHz		0.81		dB
Insertion loss[2]	100 MHz		0.37		dB
matched, up to 4.0 GHz	1.0 GHz		0.51		dB
RFC – RFx	2.0 GHz		0.68		dB
	3.0 GHz		0.81		dB
	4.0 GHz		0.89		dB
Isolation[3]	30 MHz		62		dB
unmatched	1.0 GHz		32		dB
RFC – RFx	2.0 GHz		26		dB
	3.0 GHz		22		dB
Isolation[4]	30 MHz		59		dB
unmatched, adjacent ports	1.0 GHz		29		dB
RFx – RFy	2.0 GHz		23		dB
	3.0 GHz		20		dB
Isolation, matched	100 MHz to 4.0 GHz		tbd		dB

[1] Average of the eight throws, sample ES3, 9-port measurement (Typical characteristics, published S-parameters).
[2] Average of the eight throws, matched EVB (0.3 pF shunt capacitor at RFC). Matched values are not guaranteed as they include performance of matching components. These components are beyond control of TagoreTech and therefore given values are indications, not guaranteed values.
[3] RFC to a non-active RFx port, worst case of all switch states and ports.
[4] Active RFx port to the adjacent non-active port, worst case of all switch states. Ports that are not adjacent are isolated by 4 to 6 dB more.

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Table 6: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	1		4000	MHz
Return Loss[1]	30 MHz		-29		dB
unmatched, up to 3.0 GHz	1.0 GHz		-23		dB
RFC, RFx	2.0 GHz		-19		dB
	3.0 GHz		-14		dB
Return Loss[2]	100 MHz		-28		dB
matched, up to 4.0 GHz	1.0 GHz		-21		dB
RFC, RFx	2.0 GHz		-16		dB
	3.0 GHz		-16		dB
	4.0 GHz		-26		dB

[1] Average of the eight throws, the poorer of the RFC and RFx ports, sample ES3, 9-port measurement.
[2] Matched values are not guaranteed as they include performance of matching components. These components are beyond control of TagoreTech and therefore given values are indications, not guaranteed values.

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Table 7: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	1		4000	MHz
Harmonic Distortion[1]					
H_2	30 MHz, P_{in} =40 dBm		-94		dBc
H_3	30 MHz, P_{in} =40 dBm		-89		dBc
H_2	800 MHz, P_{in} =40 dBm		-90		dBc
H_3	800 MHz, P_{in} =40 dBm		-79		dBc
IIP3	800 MHz		tbd		dBm
Power and Compression point					
P_{maxCW}	Max RF CW Power		tbd		dBm
P_{maxpeak}	Max RF Peak Power		tbd		dBm
P_{maxhot}	Max RF CW Power, hot switching		tbd		dBm
$P_{0.1\text{dB}}$[2]	30 MHz, CW		43		dBm
$P_{0.1\text{dB}}$[2]	800 MHz, CW		42		dBm
$P_{\text{peak}0.1\text{dB}}$	800 MHz, 1% duty cycle, 10μs pulse		tbd		dBm
Noise					
CP switching noise	RBW=1 kHz		tbd		dBm

[1] Average of three samples and eight throws.
[2] Average of three samples, all eight throws within 0.3 dB (Power compression). Please do not exceed Absolute Maximum ratings.

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Table 8: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	1		4000	MHz
Switching Time[1]					
t_{ON}	Switch ON time		500		ns
t_{OFF}	Switch OFF time		450		ns
t_{RISE}	Switch RISE time		250		ns
t_{FALL}	Switch FALL time		300		ns
$t_{startup}$, $C_{VCP} = 1$ nF	Start-up time		0.8		ms
Power Supply, DC					
Control voltage	Power Supply V_{DD}	2.6	3.3	5.25	V
	All control pins high[3], V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3	0	0.5	V
Bias voltage[2]	Bias pin, V_{BIAS}	-20		-18	V
Control current	All control pins high, I_{ih}			7.5	μA
	All control pins low, I_{il}		0		μA
Current consumption	I_{DD}, active mode (V_{DD} on)		240		μA

[1] Complete switching time including the internal biasing and control circuitry, internal charge pump with $C_{VCP} = 1$ nF, measured at 1 Hz and 100 Hz switching rate on three samples. Typical values include a margin of about 20 % over the measured average (Switching time definition).
[2] Bias voltage can be fed externally, or use internal charge pump. Internal charge pump produces -18 V. Please connect output of internal charge pump V_{CPOUT} to V_{BIAS} and connect CP_{DIS} to GND.
[3] Control voltage V_{ih} cannot be higher than V_{DD} (to avoid forward biasing of ESD diode).

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Switching time definition

Example of the definition by using 10 W/40 dBm signal. We apply 10W signal to RF port, stabilized with isolator. Isolator is needed as our switch shows to RF port approximately 4Ω impedance. Let's assume that the switch insertion loss is 0.3 dB. Therefore 90% of the RF signal is 39.55 dBm and 10% of the RF signal is 1W/30dBm. We need to take into account 0.3dB insertion loss, therefore numbers are 39.25 dBm and 29.7 dBm respectively. We change the control from low to high and our time reference point is when our control signal exceeds lower threshold value V_{ihlow}. In certain measurements when control signal rise time is significantly shorter than RF output signal, we approximate start of the clock with 50% point of control signal.

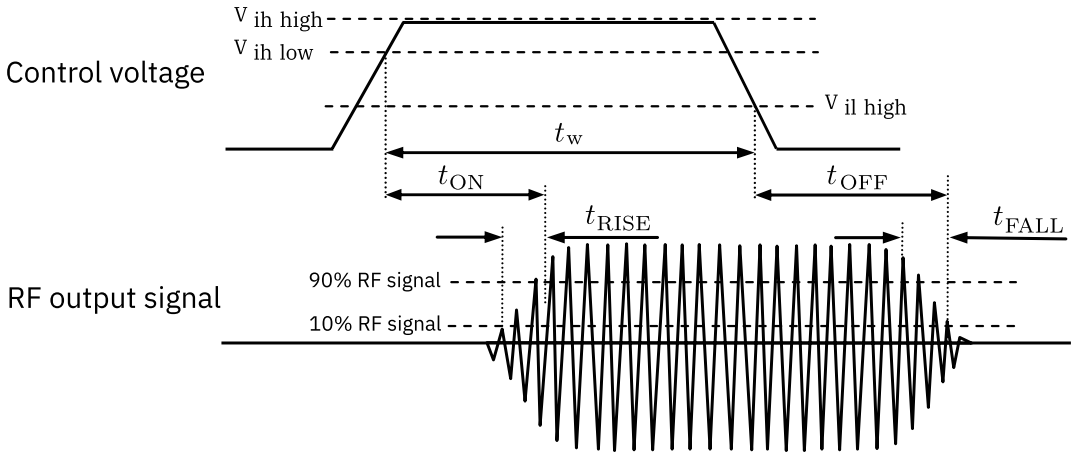


Figure 4: Switching time definition, t_{ON}, t_{OFF}, t_{RISE}, t_{FALL}.

The switching times of the TS8381M have been measured on three samples (RF1, RF4, RF5 and RF8) at 1 Hz and 100 Hz switching rate with the internal charge pump and $C_{VCP} = 1$ nF. The switching time definition includes the time of the internal biasing and control circuitry.

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Switch Control and Internal charge pump

Table 9: Switch Control Table

V_{DD}[1]	V_5[2]	V_3	V_2	V_1	**Switch state**
1	0	0	0	0	RFC – RF1 ON
1	0	0	0	1	RFC – RF2 ON
1	0	1	1	0	RFC – RF3 ON
1	0	1	1	1	RFC – RF4 ON
1	0	1	0	0	RFC – RF5 ON
1	0	1	0	1	RFC – RF6 ON
1	0	0	1	0	RFC – RF7 ON
1	0	0	1	1	RFC – RF8 ON
1	1	0	0	0	RFC – RF8 ON (flipped)
1	1	0	0	1	RFC – RF7 ON (flipped)
1	1	1	1	0	RFC – RF6 ON (flipped)
1	1	1	1	1	RFC – RF5 ON (flipped)
1	1	1	0	0	RFC – RF4 ON (flipped)
1	1	1	0	1	RFC – RF3 ON (flipped)
1	1	0	1	0	RFC – RF2 ON (flipped)
1	1	0	1	1	RFC – RF1 ON (flipped)
0	0	0	0	0	V_{DD} off (Isolation), all FETs are on, short shown to RFC and RFx ports

[1] V_{DD} should be applied first before V_1, V_2, V_3 and V_5, otherwise may cause damage to the device.
[2] V_5 is a flip bit. With V_5 high the control table is mirrored: the control word of RF1 selects RF8, RF2 selects RF7, RF3 selects RF6 and so on. The RF performance has been characterized with V_5 low.

Internal Charge Pump

TS8381M has an internal charge pump, which can be disabled with the CP_{DIS} pin by connecting it to V_{DD}. Using the internal charge pump, please connect V_{CPOUT} to V_{BIAS} and CP_{DIS} to GND.

As there might be some noise from the charge pump below 250 MHz, it is recommended for frequencies below 250 MHz to disable the charge pump by connecting the CP_{DIS} pin to V_{DD} and to feed -18 V...-20 V to the V_{BIAS} pin. This ensures noise free operation below 250 MHz.

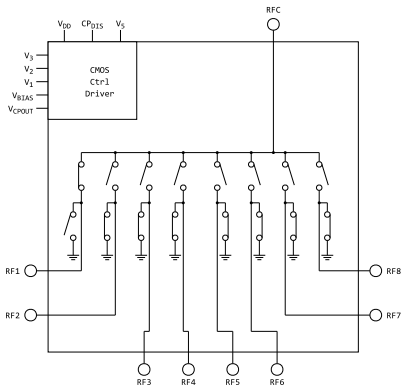
Option 1: Use internal charge pump

- Connect CP_{DIS} pin to GND.
- Connect V_{CPOUT} to V_{BIAS}.

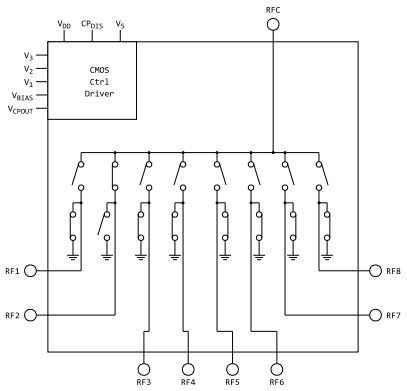
Option 2: Use external negative voltage -18 V...-20 V, charge pump OFF

- Connect CP_{DIS} pin to V_{DD}.
- Connect V_{CPOUT} pin to GND.
- Feed -18 V...-20 V to V_{BIAS} pin.

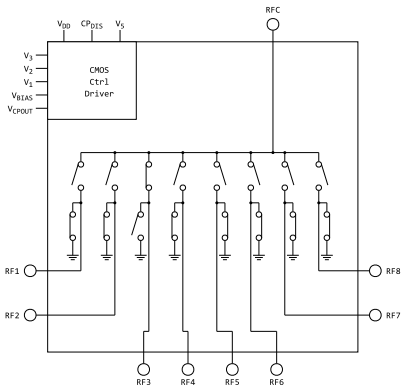
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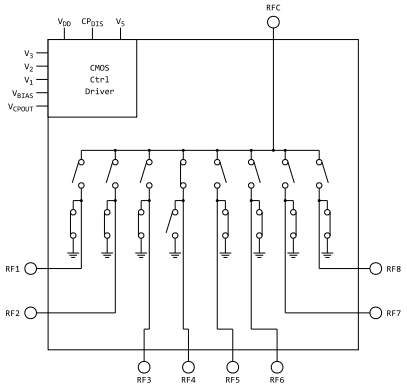
RFC-RF1 ON



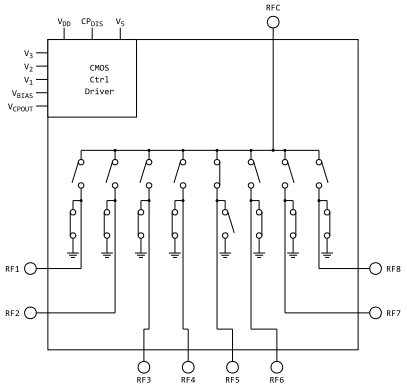
RFC-RF2 ON



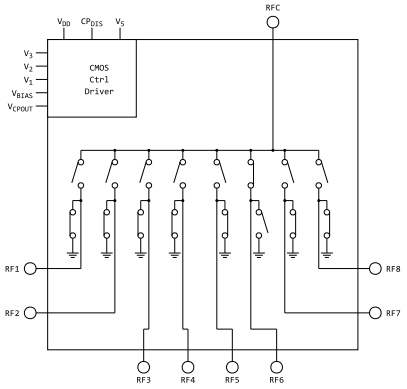
RFC-RF3 ON



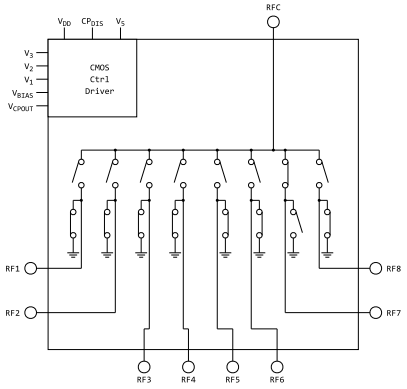
RFC-RF4 ON



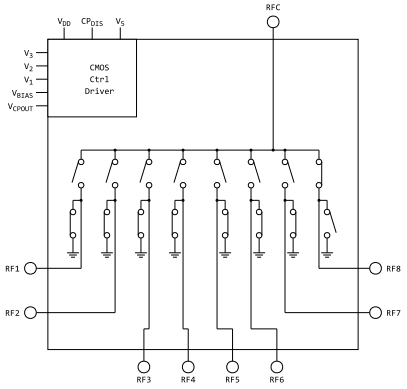
RFC-RF5 ON



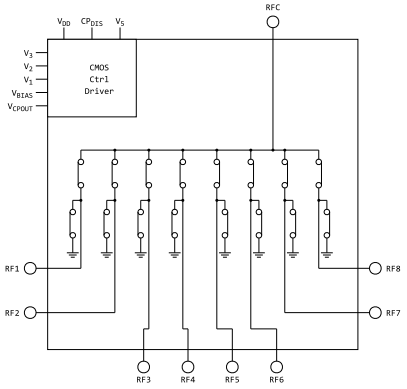
RFC-RF6 ON



RFC-RF7 ON



RFC-RF8 ON



V_{DD} off state

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Theory of Operation

Switch topology

Each throw of the TS8381M consists of a series switch between RFC and the RFx port and a shunt switch from the RFx port to ground. In the ON state of a throw, its series switch is closed and its shunt switch is open; the non-active throws have the series switch open and the shunt switch closed, so that the non-active RFx ports show a short to ground (reflective switch).

Flip bit V_5

With V_5 low, the control words $V_3V_2V_1$ select the throws as in the Switch Control Table. With V_5 high, the table is mirrored: the control word of RF1 selects RF8, RF2 selects RF7, RF3 selects RF6, RF4 selects RF5, and vice versa. The flip bit allows mirrored layouts with the same control word, see Application Information.

Device powered off

When V_{DD} is 0 V, all switch RF transistors are on, i.e. both the series and the shunt transistors are conducting. Every RF port is essentially connected to ground, including the RFC port (measured 1.5 Ω at RFC and 2.5 Ω at the RFx ports at 100 MHz, RFC − RFx isolation 33 dB at 100 MHz and 27 dB at 1 GHz). This is practical when device is directly connected to the antenna, there is certain protection against induced electrical fields when the device is not in usage.

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Application Information

TS8381M is a 15 W single pole eight throw switch for 1 MHz to 4000 MHz. Applications include switched filter banks, delay line banks and band selection in narrowband and multi-octave wideband radios, jammers, EMC testing, public mobile radios, industrial and scientific applications. TS8381M works well up to 3.0 GHz without external matching components; for frequencies above 3.0 GHz, matching is recommended. The datasheet provides an example matching (one shunt capacitor at the RFC port) and its performance.

In a filter bank, delay line bank or any similar bank of components, one TS8381M is used at each end of the bank. The two switches face each other and are mirrored: RF1 of the input switch connects to RF8 of the output switch, and so on. With V_5 low on one switch and high on the other (flip bit), both switches share the same control lines, and a single control word $V_3V_2V_1$ selects the filter, delay line or other component of the bank.

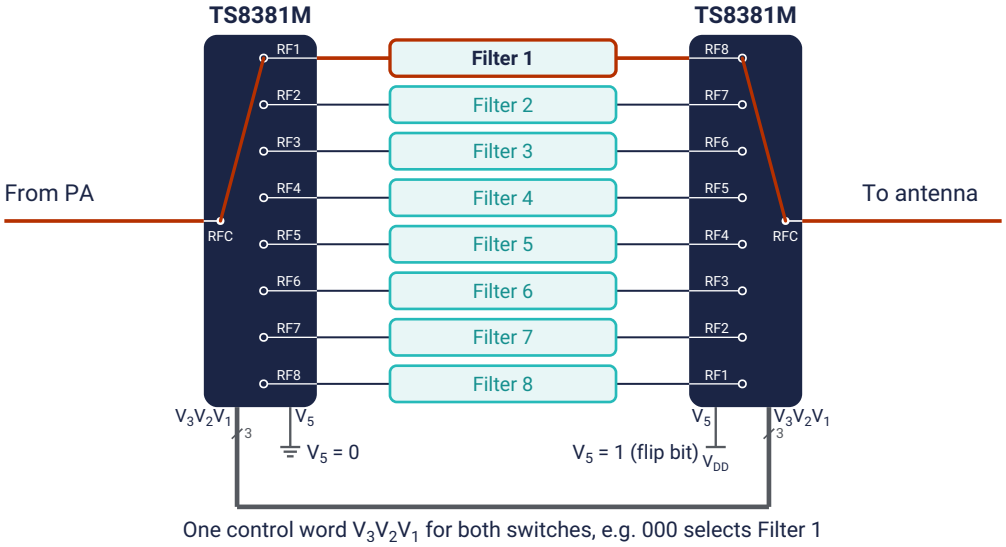


Figure 6: Filter bank with two TS8381M switches. The output switch has V_5 = 1 (flip bit), so both switches use the same control word: $V_3V_2V_1$ = 000 selects RF1 of the input switch and RF8 of the output switch, i.e. Filter 1. The same applies to delay line banks or any similar bank of components.

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Schematics and Evaluation Board

S-parameters of the unmatched EVB can be downloaded from this link: Download TS8381M S-parameters

Table 10: Port definitions in s-parameter files and plots.

PIN name	Pin	Port number	Function
RFC (ANT)	41	9	RF common port, S99
RFx	9, 12, 14, 17, 20, 23, 25, 28	1 ...8	RF port x (x = 1 ...8), Sxx
RFxON			RFC-RFx ON, Sx9

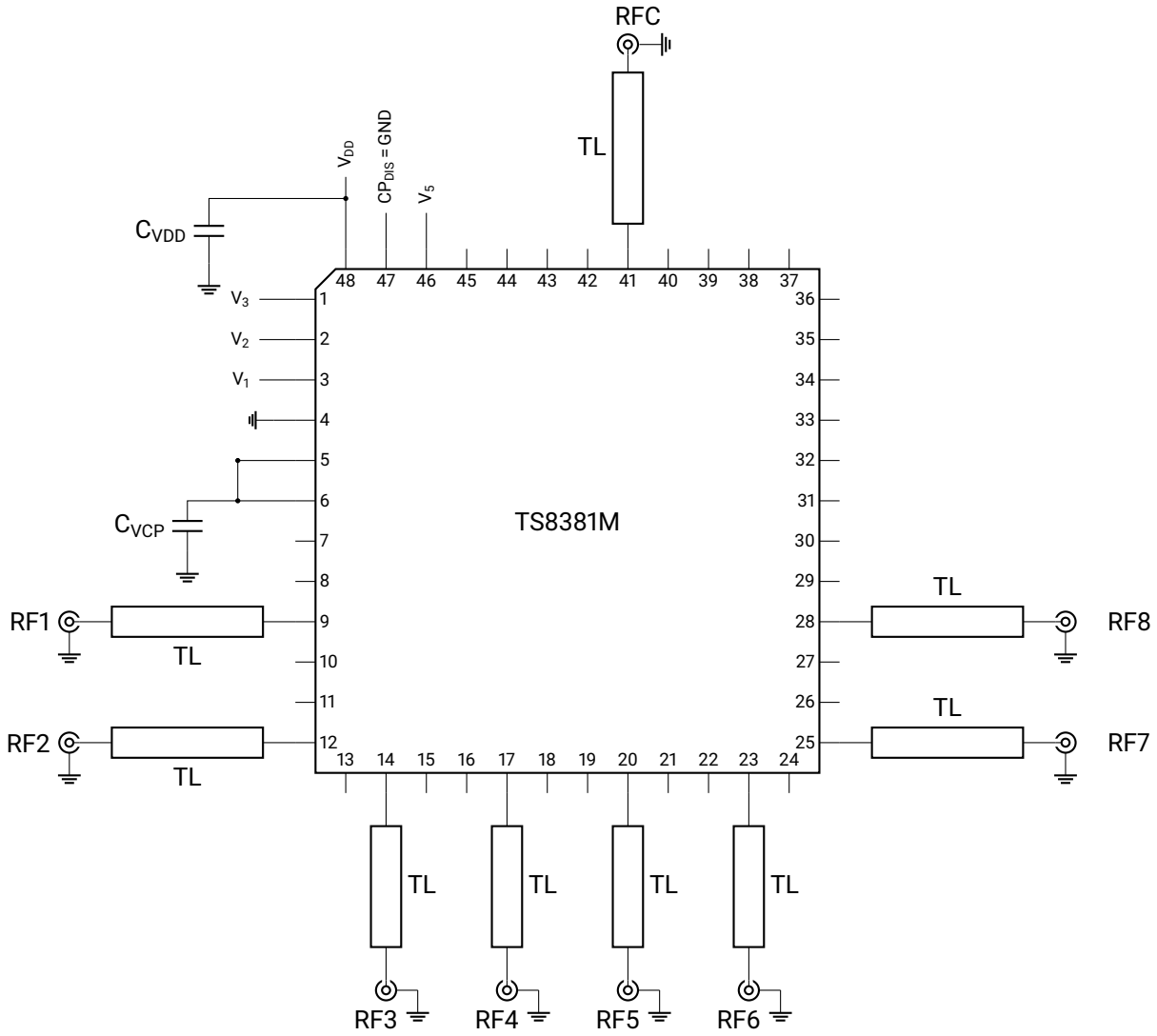
Content of s-parameter repository:

```
TS8381M.zip
└─ TS8381M_IDX_00 ..... s-parameters without matching components
   ├─ Readme.txt
   ├─ TS8381M_RF1ON_9PORT.s9p ..... S9P file for RFC-RF1 ON mode
   ├─ TS8381M_RF2ON_9PORT.s9p ..... S9P file for RFC-RF2 ON mode
   ├─ ...
   ├─ TS8381M_RF8ON_9PORT.s9p ..... S9P file for RFC-RF8 ON mode
   └─ TS8381M_VDDOFF_9PORT.s9p ..... S9P file for V_DD off
```


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Performance up to 3.0 GHz, unmatched

TS8381M shows best performance up to 3.0 GHz frequency without any matching components. Only two external components are recommended, 1 nF for V_{CPOUT}/V_{BIAS} and 10 nF for V_{DD} lines for supporting charge pump and power supply.



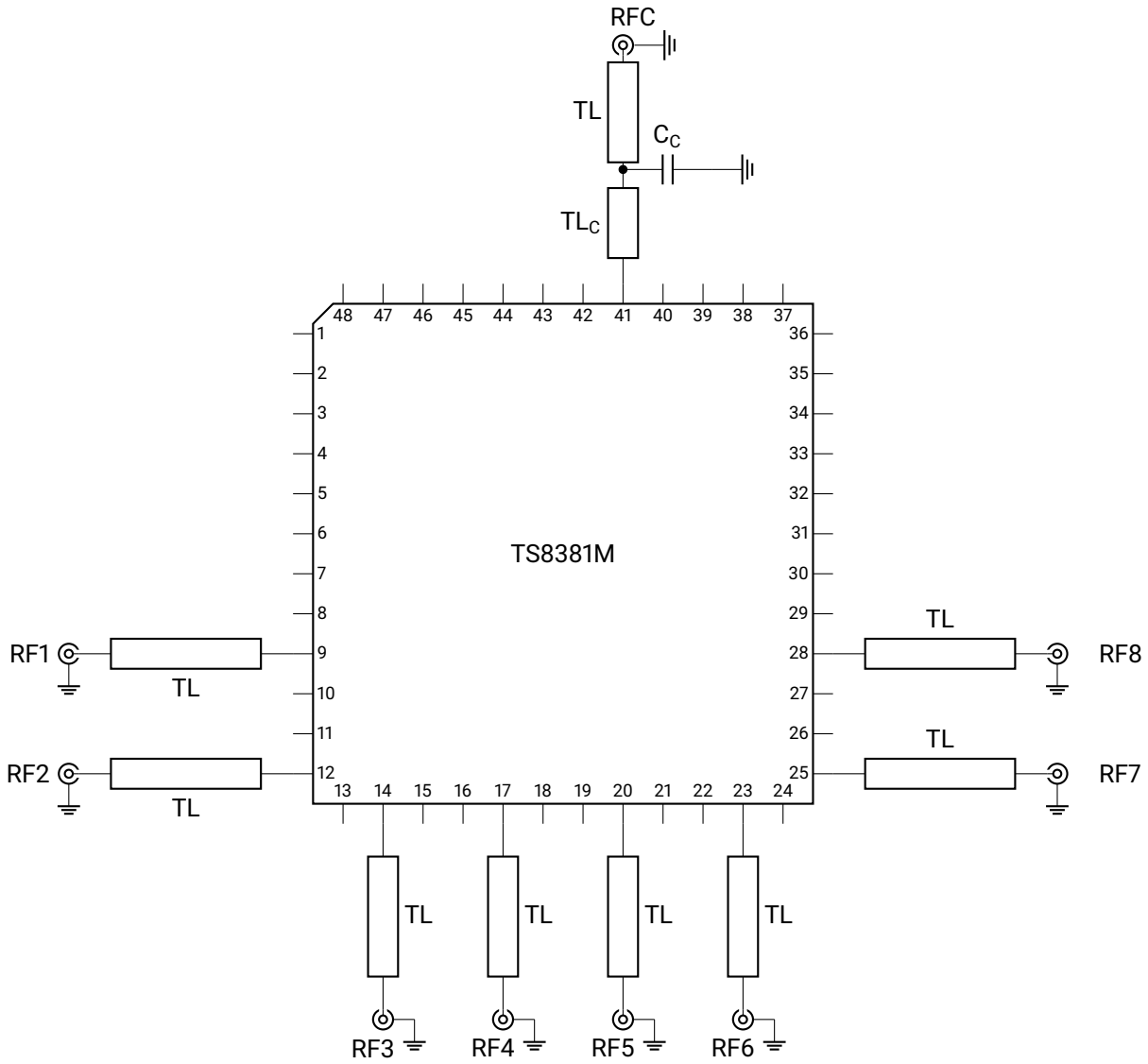
Schematics of TS8381M EVB, internal charge pump (V_{CPOUT} connected to V_{BIAS}, CP_{DIS} to GND). The unused GND/NC pins and the thermal pad are grounded.

Table 11: Components used for TS8381M EVB

Reference	Part number / Value	Description	Notes
C_{VDD}	10 nF	Capacitor	GRM155R71H103KA88
C_{VCP}	1 nF	Capacitor	GRM155R71H102KA01D

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Performance up to 4.0 GHz, matched



Schematics of the matched TS8381M EVB (RF part; supply and control as the unmatched EVB).

Table 12: Matching components used for 4.0 GHz matching

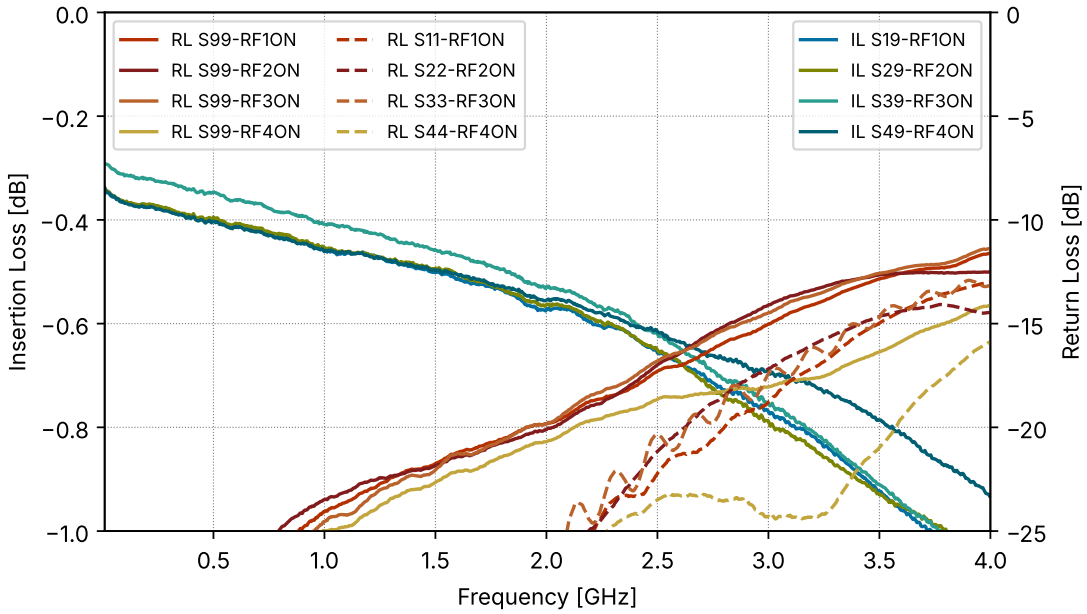
Reference	Part number / Value	Description	Notes
TL_C	6.5 mm	Transmission line	Series line from the RFC pin to the capacitor
C_C	ATC00S0R3BT	Ceramic capacitor	0.3 pF shunt capacitor
C_{VDD}	10 nF	Capacitor	GRM155R71H103KA88
C_{VCP}	1 nF	Capacitor	GRM155R71H102KA01D

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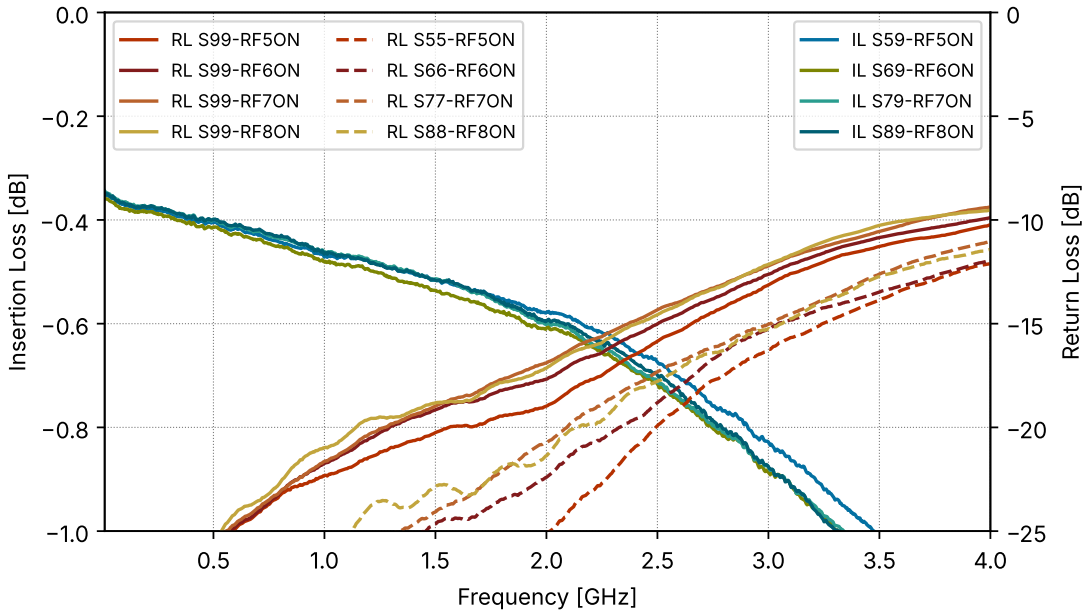
Typical characteristics

Performance up to 3.0 GHz, unmatched

These measurements have been taken from TS8381M EVB (sample ES3) with a 9-port vector network analyzer; they are the published S-parameters. Device does not require any matching components for operation up to 3.0 GHz. Going above 3.0 GHz, performance can be improved by adding matching to the RFC port. Our matching example shows good performance up to 4.0 GHz.

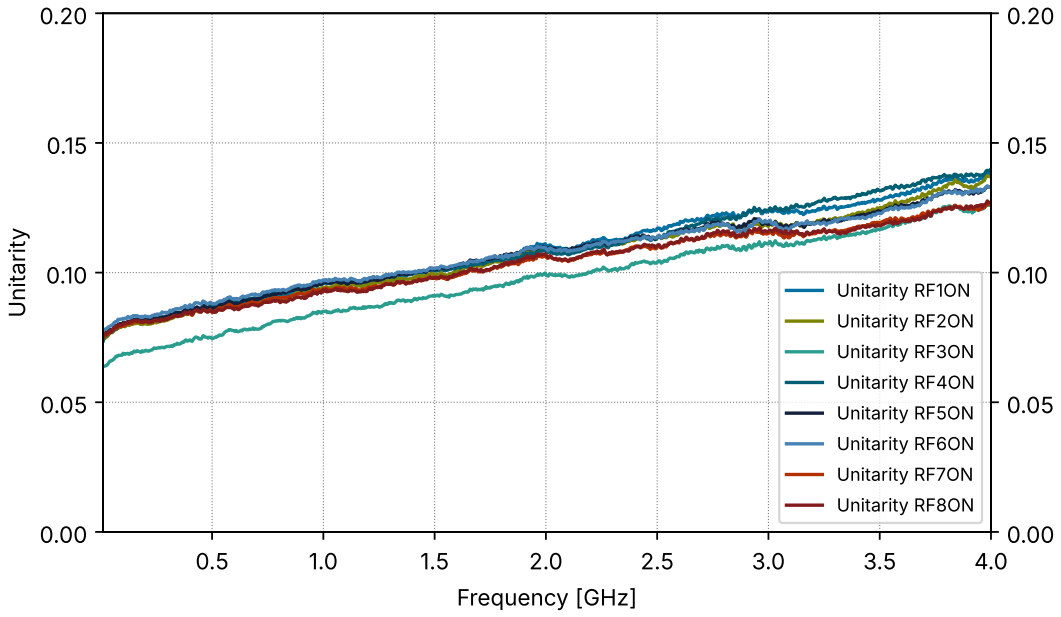


Insertion loss and Return loss, RFC – RFx, RF1 to RF4.

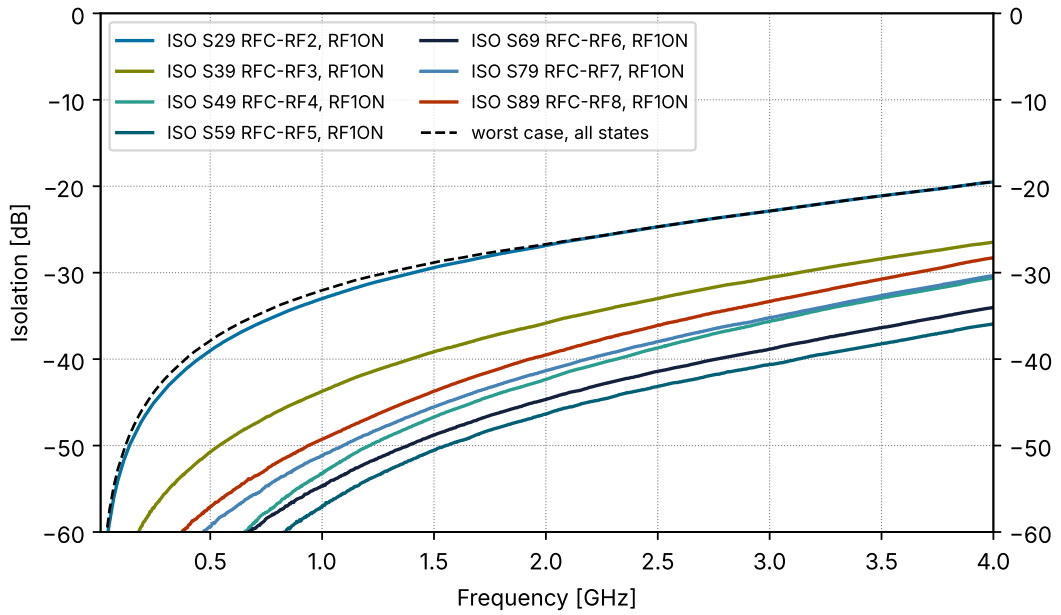


Insertion loss and Return loss, RFC – RFx, RF5 to RF8.

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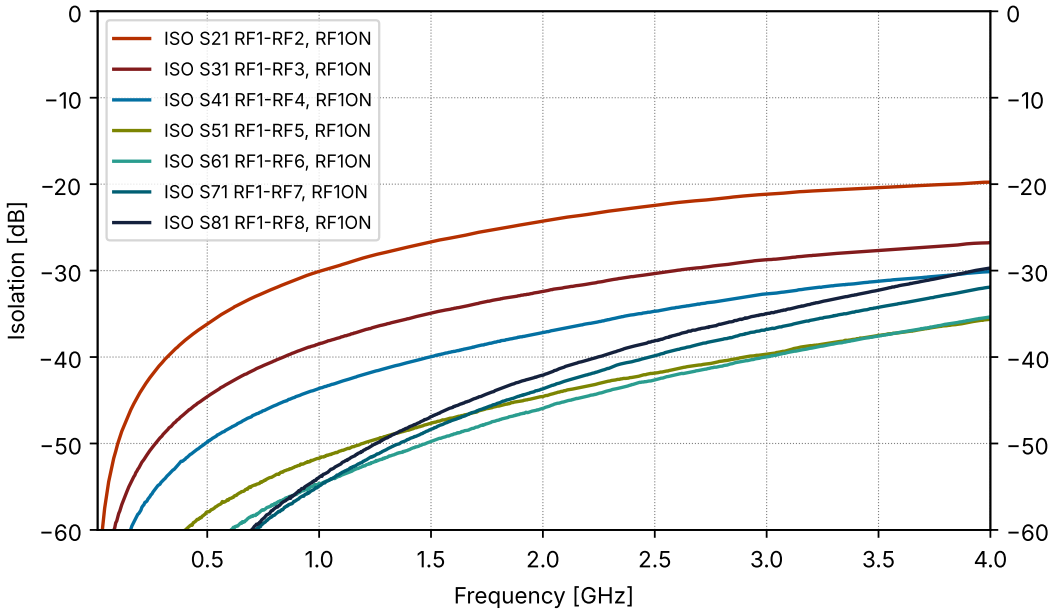


Power absorption of the switch $1 - \sum_{k=1}^{9} |S_{k9}|^2$, RFC − RFx ON, RFC (port 9) input.

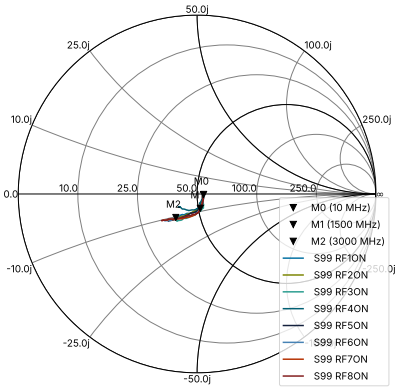


Isolation between RFC and the non-active RFx ports, RF1 ON, and the worst case of all switch states (dashed).

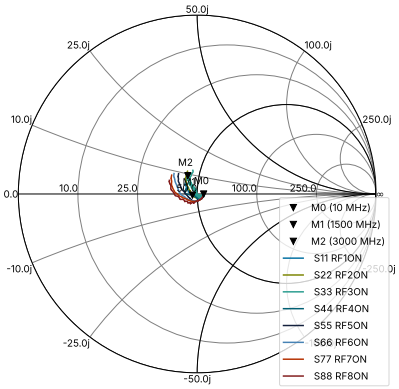
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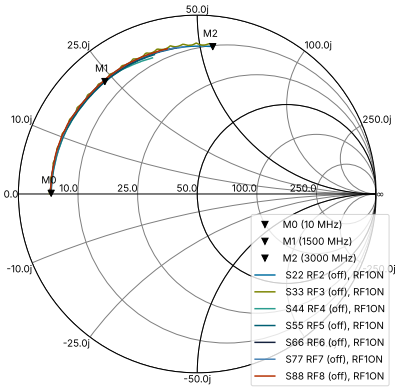
RFx – RFx port isolation, RF1 ON: active RF1 to the non-active ports. The adjacent port RF2 is the least isolated.



RFC matching at ON state.



RFx matching at ON state.

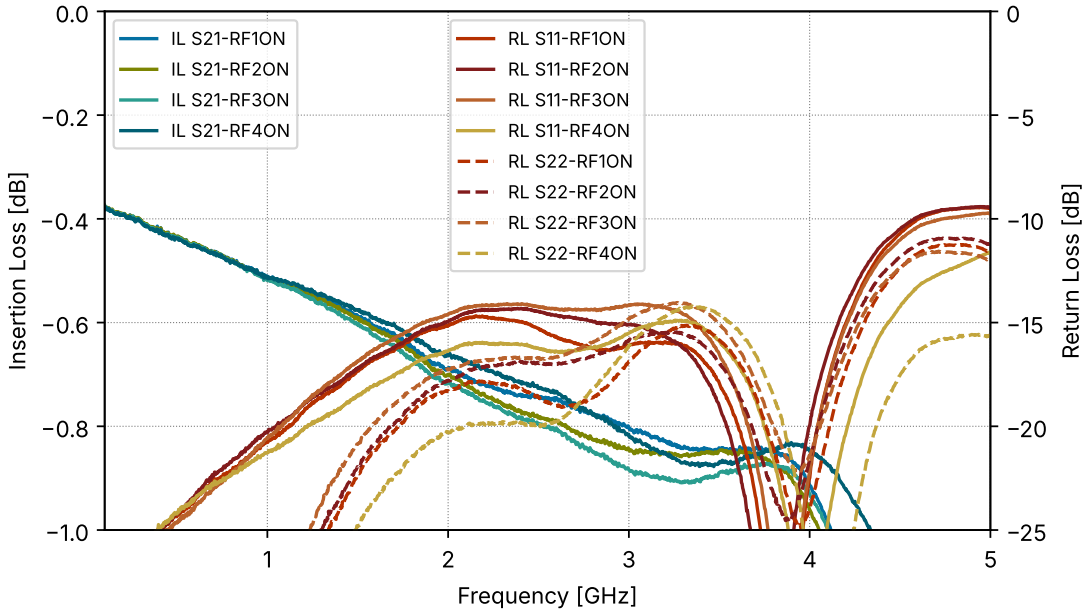


Non-active RFx port impedance, RF1 ON. Low frequency starts from closed (short) and circulates towards open at higher frequencies.

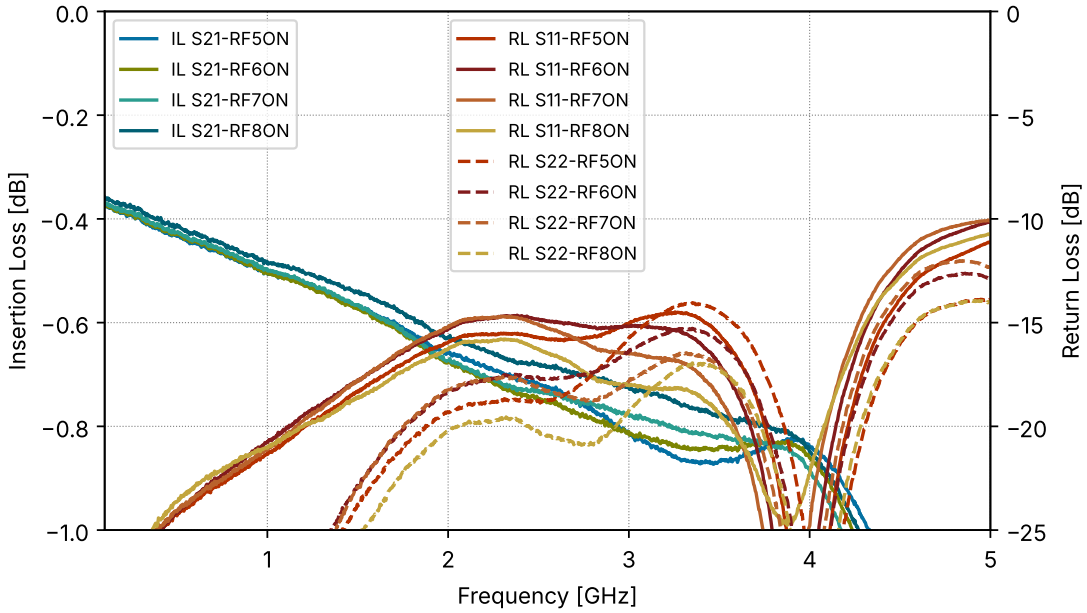
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Performance up to 4.0 GHz, matching applied to EVB

These measurements have been taken from the matched TS8381M EVB (6.5 mm line and 0.3 pF shunt capacitor at RFC), matching component losses are present. Isolation data and the downloadable S-parameters of the matched EVB will be added later.

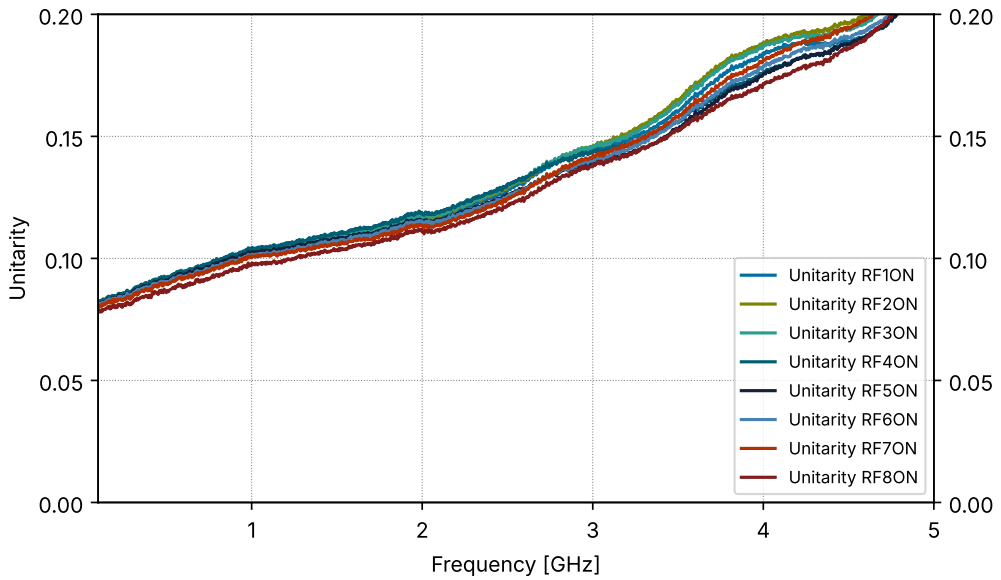


Insertion loss and Return loss, RFC – RFx, RF1 to RF4, matched.

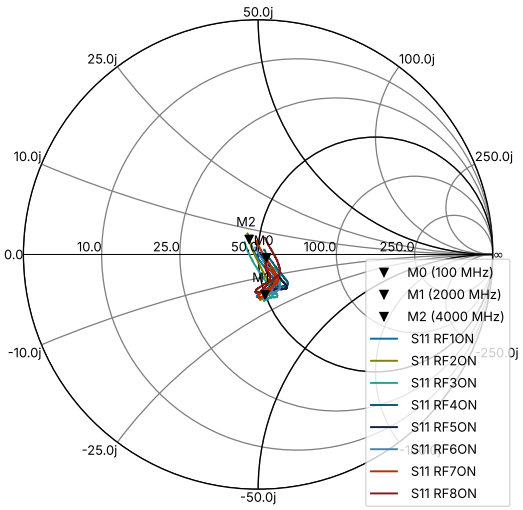


Insertion loss and Return loss, RFC – RFx, RF5 to RF8, matched.

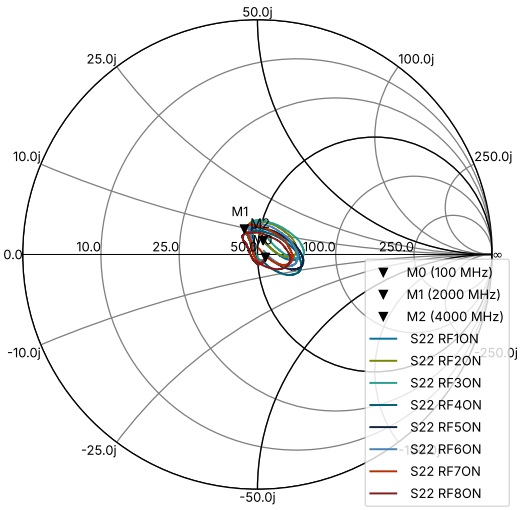
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Power absorption of the switch $1 - |S_{11}|^2 - |S_{21}|^2$, RFC – RFx ON, matched.



RFC matching at ON state, matched.

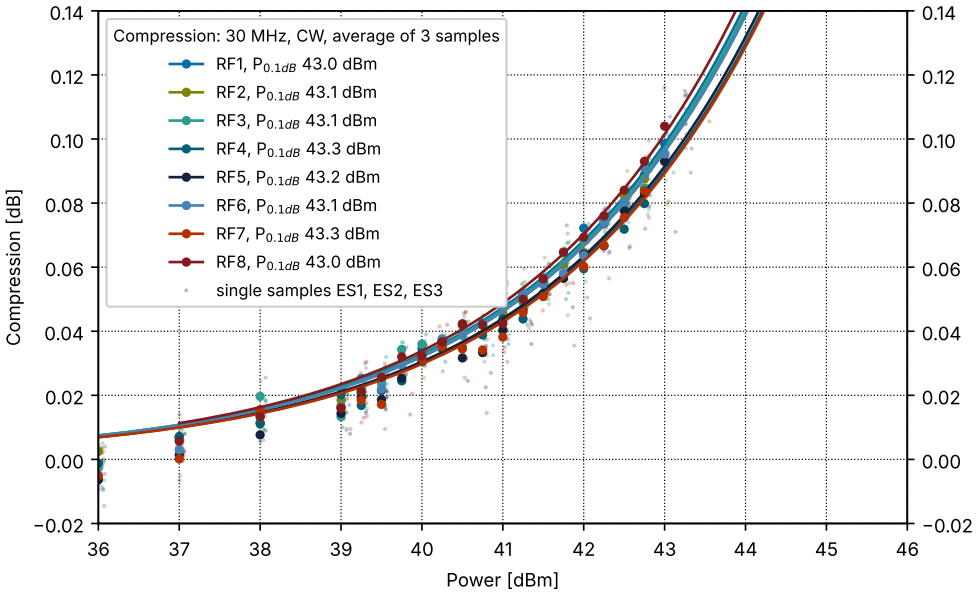


RFx matching at ON state, matched.

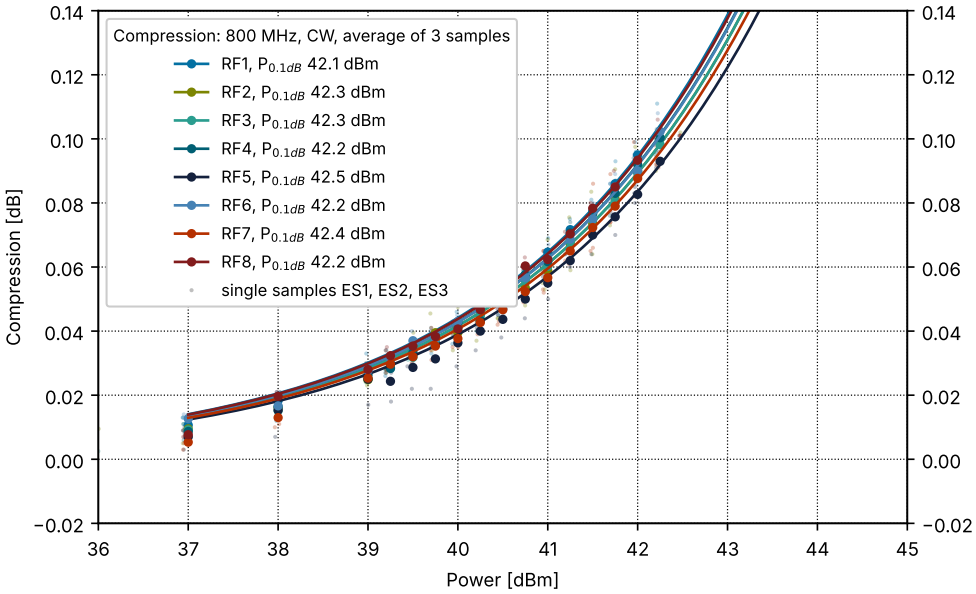
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Power compression

TS8381M Continuous Wave (CW) compression measurements are presented for 30 MHz and 800 MHz, three samples and all eight throws. Measurements are conducted in room temperature $T_A = +25$°C. Measurements of the average of three samples are presented as dot (•), single samples as small light dots, and model and extrapolations presented as line (−). Power derating and maximum power ratings are tbd.



TS8381M CW compression at 30 MHz in room temperature $T_A = +25$°C.



TS8381M CW compression at 800 MHz in room temperature $T_A = +25$°C.

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Device Package information

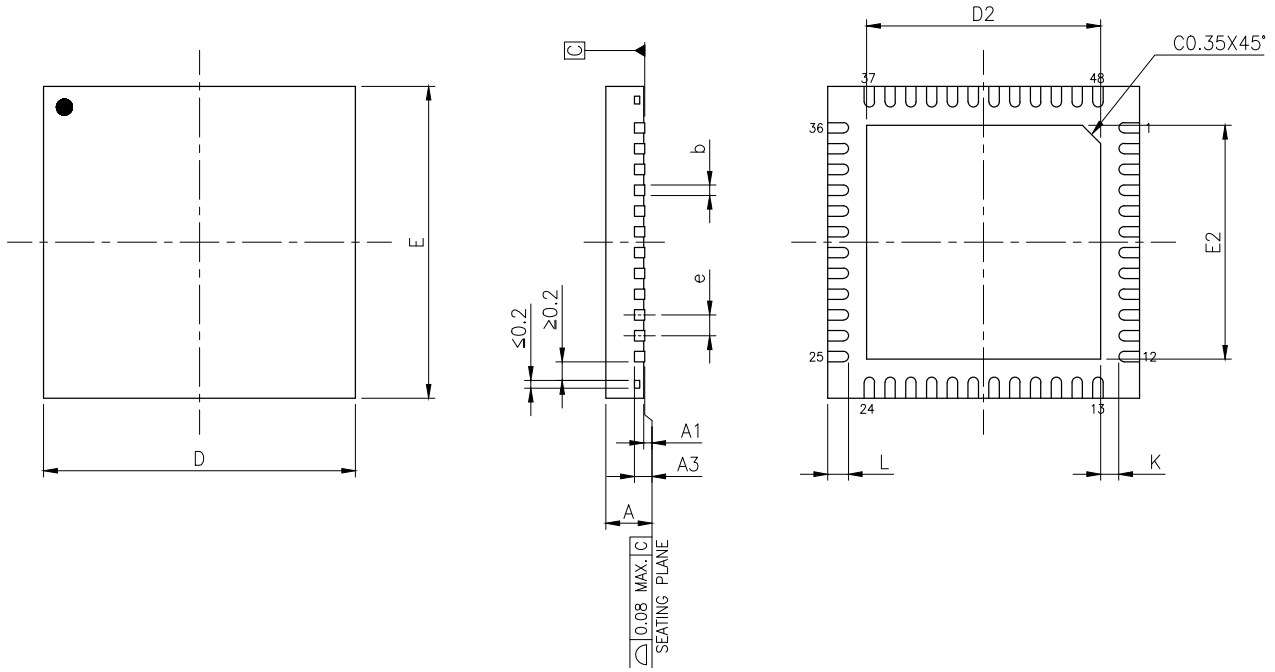


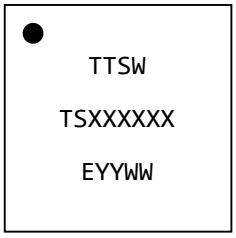
Figure 9: 48-pin QFN 6.0 x 6.0 x 0.85 mm^3 package drawing, top view, side view and bottom view.

Please refer to application notes TN-001 PCB Design guideline and TN-002 Solder Rework at TagoreTech web page for PCB and soldering guidelines.

Table 13: Device Package Dimensions

Dimension	Min [mm]	Nom [mm]	Max [mm]	Dimension	Min [mm]	Nom [mm]	Max [mm]
A	0.80	0.85	0.90	D2	4.45	4.50	4.55
A1	0.00	0.02	0.05	E2	4.45	4.50	4.55
A3	0.203 REF			L	0.35	0.40	0.45
b	0.15	0.20	0.25	e	0.40 BSC		
D	6.00 BSC			K	0.20	–	–
E	6.00 BSC			Pin 1 corner of the exposed pad: C0.35×45°			

All dimensions are in millimeters. Dimension b applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. Coplanarity 0.08 mm max., applies to the exposed heat sink slug as well as the terminals.



●	Pin 1 indicator
TTSW	TagoreTech SWitch
TSXXXXXX	Part number (8 digits max)
E	Fixed letter before date code
YY	Last two digits of assembly year
WW	Assembly work week

Figure 10: Part marking specification.

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PCB Land Design

Notes:

- 4-layer PCB is recommended.
- Via diameter is recommended to be 0.3mm to prevent solder wicking inside the vias.
- Thermal vias shall only be placed on the center pad.

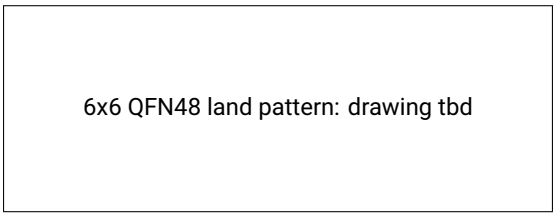


Figure 11: PCB land pattern, dimensions in [mm].

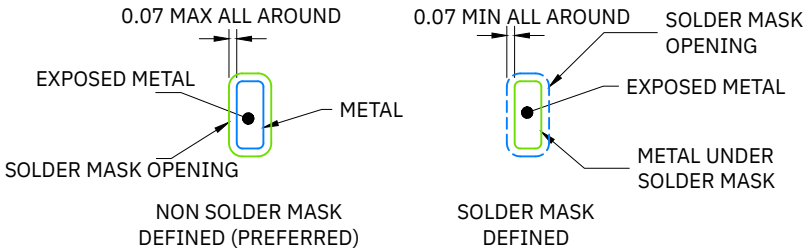


Figure 12: Solder mask opening, dimensions in [mm].

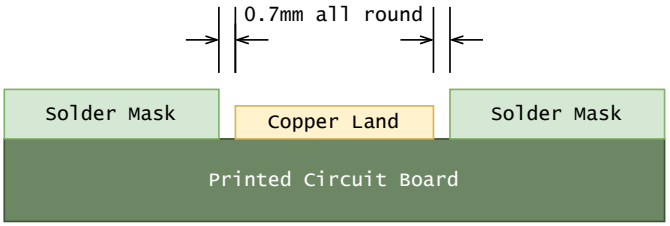


Figure 13: Preferred solder mask opening, side view, dimensions in [mm].

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PCB Stencil Design

Notes:

- Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- Stencil thickness is recommended to be 125 μm.

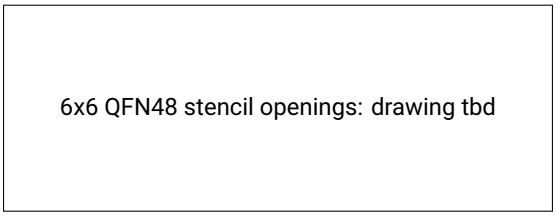
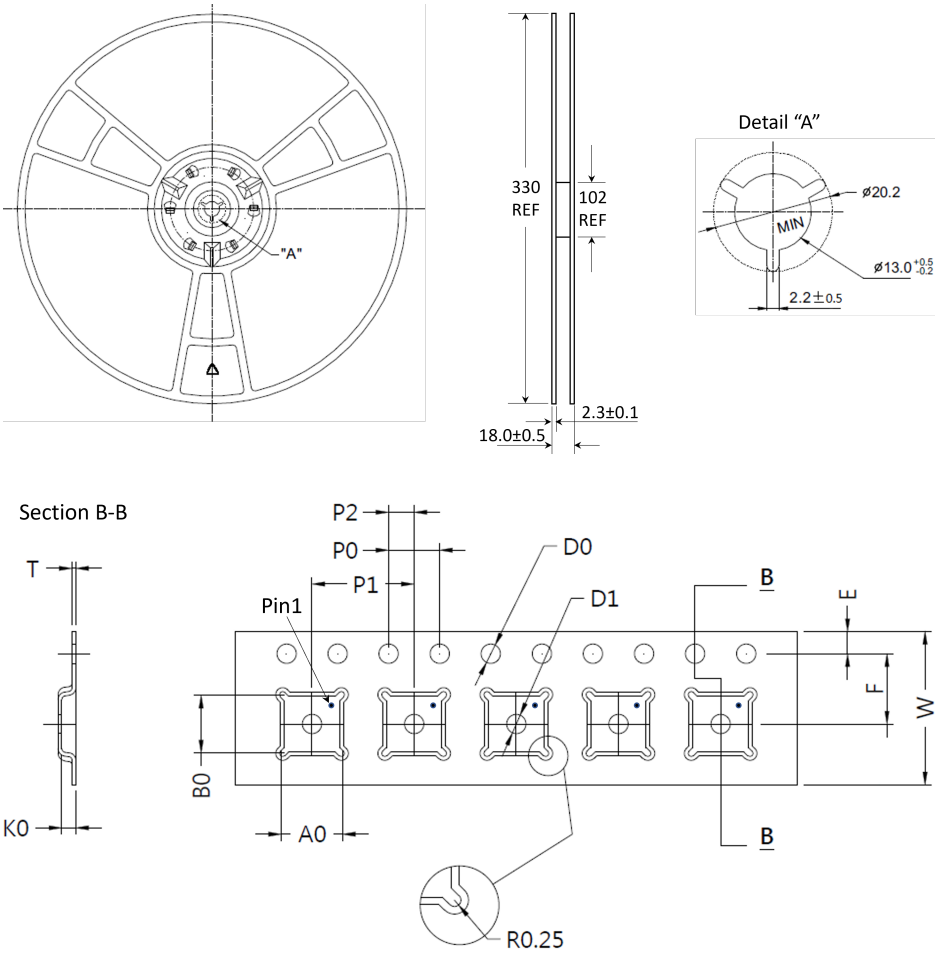


Figure 14: Stencil Openings, dimensions in [mm].

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Tape and Reel Information



A0[mm]	B0[mm]	D0[mm]	D1[mm]	E[mm]	F[mm]	K0[mm]	P0[mm]	P1[mm]	P2[mm]	T[mm]	W[mm]
tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd

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Glossary

IL	Insertion loss
ISO	Isolation
RL	Return loss
VSWR	Voltage Standing Wave Ratio
RFC (ANT)	RF common port (antenna port, pin 41)
RFx	RF Port number x
V_{BIAS}, V_{CPOUT}, CP_{DIS}	Bias voltage input, charge pump output, charge pump disable
Unitarity	Describes power absorption of the component, $1 - \sum_k \lvert S_{k9} \rvert^2$ (port 9 = RFC)
EVB	Evaluation board

Changelog

Table 14: Changelog

Date	Revision	Notes
11/08/2026	0.50	Preliminary Datasheet, first publication.
11/09/2026	0.51	V_5 defined as flip bit: mirrored switch control table, pin definition, features, theory of operation and application information (filter and delay line banks) with a filter bank figure. Package render on the first page. Marketing name 15 W switch in the title.

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TS8381M Product information

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Latest version of TS8381M datasheet is available for download: TS8381M Datasheet

S-parameters of the TS8381M (unmatched EVB) are available: TS8381M S-parameters

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