TS8441L - 30W CW GaN Broadband RF Switch SP4T

1.0 Features

- Low insertion loss: 0.2dB @ 800MHz
- High isolation: 38dB @ 800MHz
- 30W CW power handling capability
- No external DC blocking capacitors on RF lines
- Operating frequency: 30MHz to 4.0GHz
- Versatile 2.6-5.25V power supply

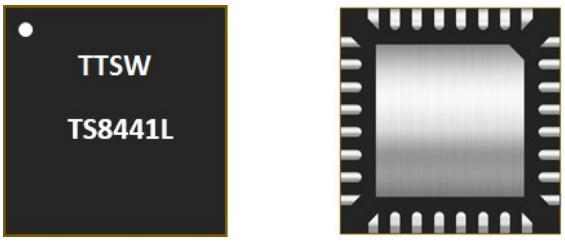


Figure 1 Device Image
(32 Pin 4×4×0.8mm QFN Package)

2.0 Applications

- Private mobile radio handsets
- Public safety handsets
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Satellite terminals

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS8441L is a symmetrical reflective Single Pole Four Throws (SP4T) switch designed for broadband, high power switching applications. Its broadband behavior from 30MHz to 4.0GHz frequencies makes the TS8441L an excellent switch for all the applications requiring low insertion loss, high isolation, and high linearity within a small package size.

The TS8441L is packaged into a compact Quad Flat No lead (QFN) 4x4mm 32 leads plastic package.

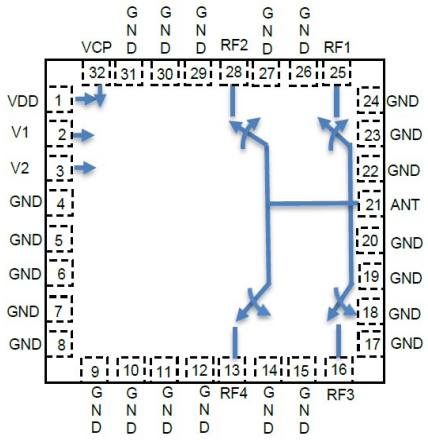


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1a Ordering Information

Device Part Number	Package Type	Eval Board Part Number
TS8441L	32 Pin 4×4×0.8mm QFN	TS8441L-EVB

Table 1b Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3,000	13” (330mm)	18mm

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	VDD	DC power supply
2	V1	Switch control input 1
3	V2	Switch control input 2
4,5,6,7,8,9,10,11,12,14,15,17, 18,19,20,22,23,24,26,27,29,30,31	NC	No internal connection, can be grounded
13	RF4	RF port 4
16	RF3	RF port 3
21	ANT	Antenna port
28	RF2	RF port 2
25	RF1	RF port 1
32	VCP	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time.

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	5.5	V
Storage Temperature Range	T_{st}	-55 to +125	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+140	°C
Maximum RF input power(400MHz~4000MHz)	RFx/ANT	45	dBm
Maximum RF input power(30MHz~400MHz)	RFx/ANT	43	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	25	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$	≤ 37	°C/W

Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+3.3V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating Frequency		30		4000	MHz
Insertion Loss, RFx	400MHz		0.18		dB
	800MHz		0.22	0.45	
	1.95GHz		0.3		
	2.5GHz		0.35		
	4.0GHz		1.0		
Isolation, ANT-RFx	400MHz		45		dB
	800MHz	34	38		
	1.95GHz		29		
	2.5GHz		26		
	4.0GHz		20		
Return Loss, ANT-RFx	400MHz		35		dB
	800MHz		30		
	1.95GHz		20		
	2.5GHz		17		
	4.0GHz		10		
H2	800MHz, Pin=42dBm		80		dBc
H3	800MHz, Pin=42dBm		77		dBc
IIP3	800MHz		70		dBm
P0.1dB[1]	800MHz, 1% duty cycle, 1mS period		48		dBm
	800MHz, CW	45	47		dBm
	30MHz, CW	43			dBm
Switching time	50% ctrl to 10/90% of the RF value is settled. C1=1nF (refer to Figure 3)		0.8		μs
Control Voltage	Power supply VDD	2.6	3.3	5.25	V
	All control pins high, V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control Current	All control pins low, I_{il}		0		μA
	All control pins high, I_{ih}			7.5	μA
Current Consumption, IDD	Active mode		160	200	μA

Note: [1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	V2	Active RF Path
0	0	ANT-RF1
1	0	ANT-RF2
0	1	ANT-RF3
1	1	ANT-RF4

Attention:
[1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.
[2] There is an internal pull-down to ground on V1 and V2 control pins, therefore the switch state at start-up without any control voltage applied will be ANT-RF1 on by default.

9.0 Evaluation Board Schematic

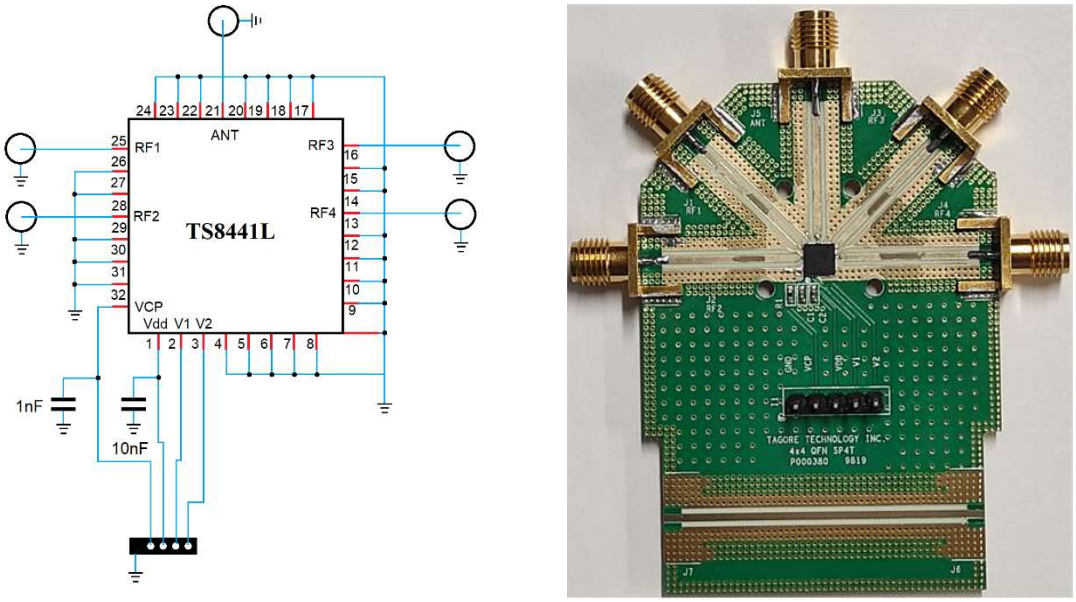


Figure 3 Evaluation Board and Schematic

10.0 Typical Electrical Characteristics

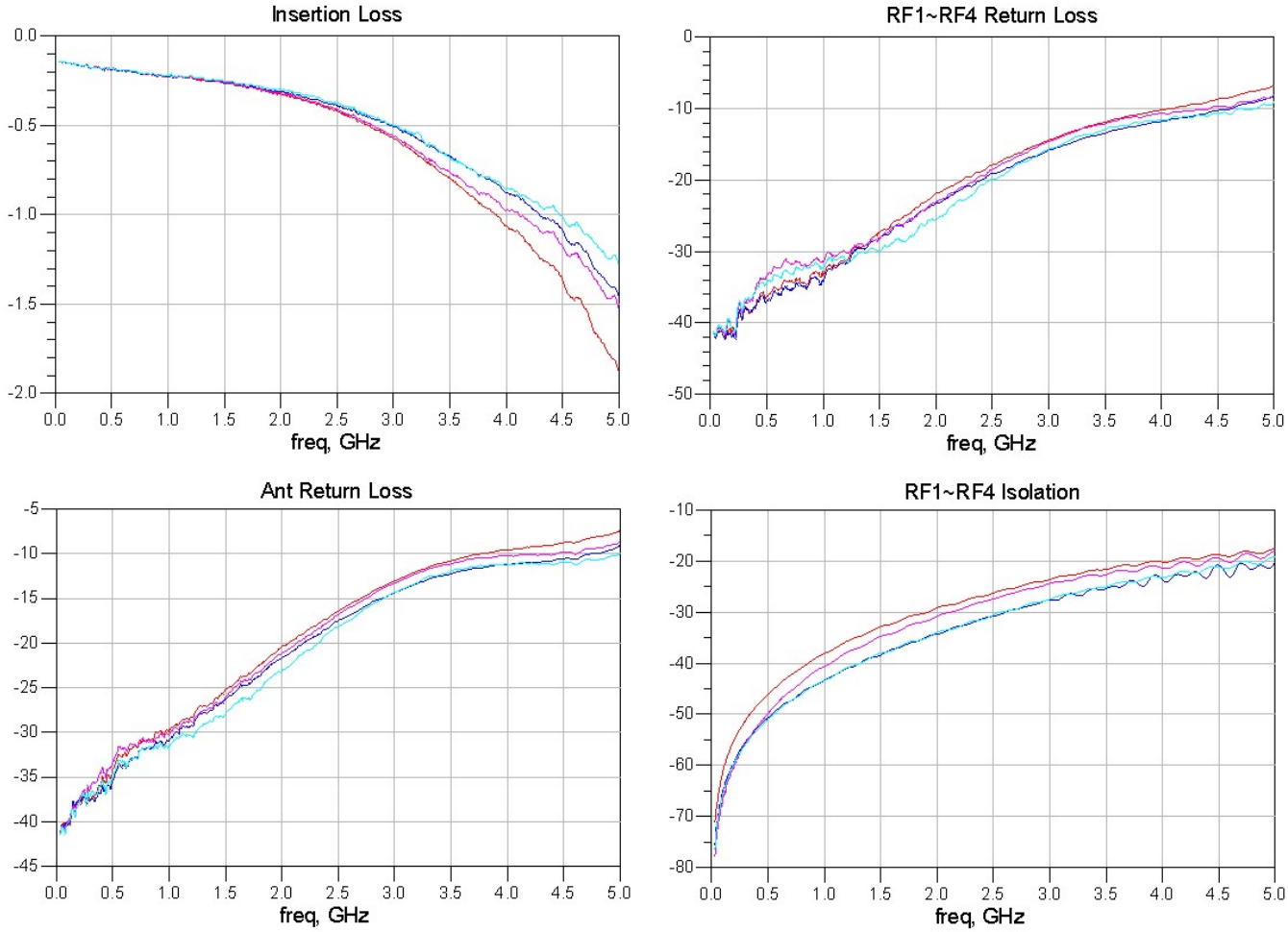


Figure 4 Typical Small Signal Characteristics (No Match)

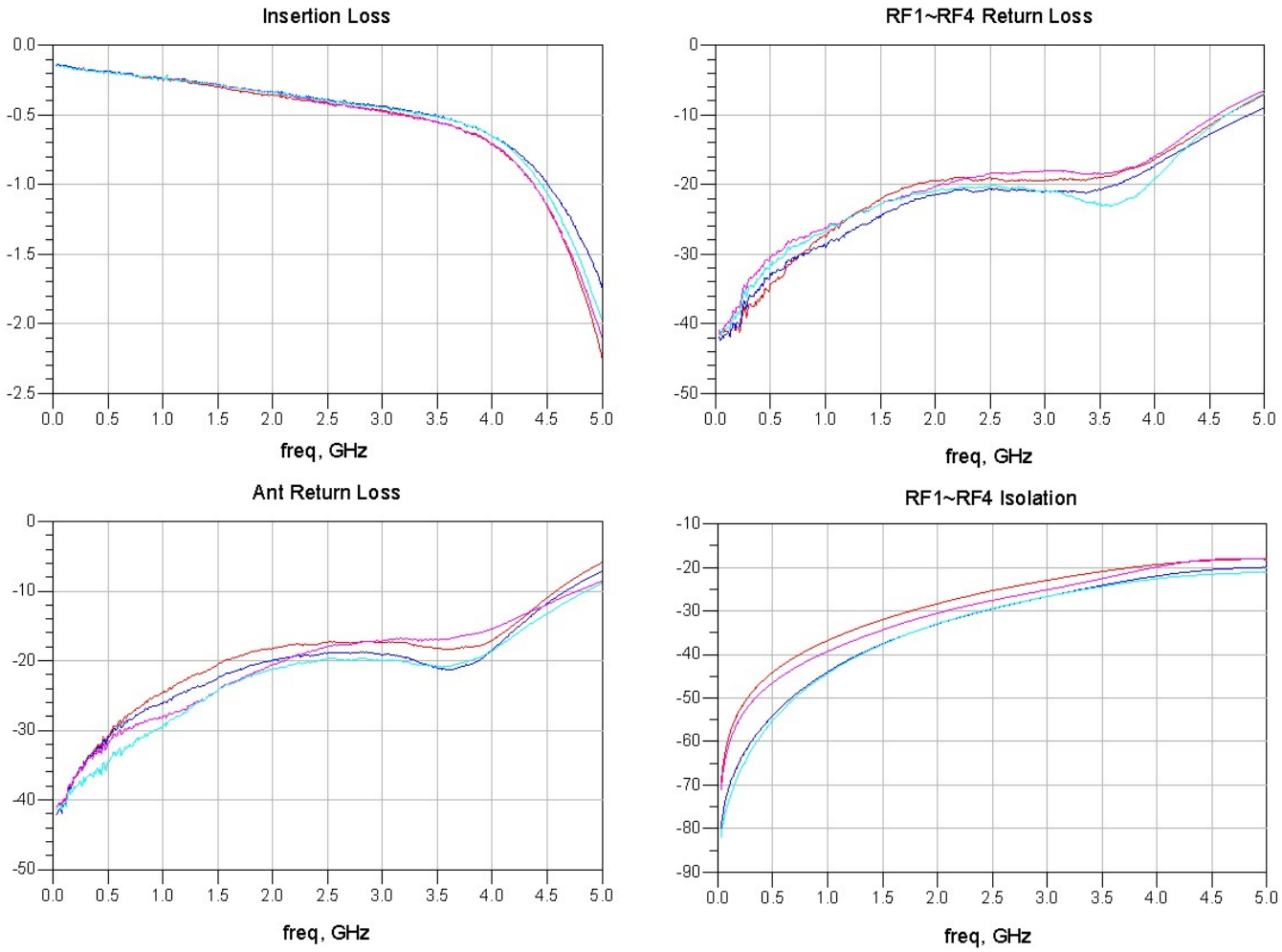


Figure 5 Typical Small Signal Characteristics (Matched [1])

[1] Matching circuit: at pin ANT port, add 1nH series inductor followed by 0.4 pF shunt capacitor

Table 6 Recommended Evaluation Board Component Values

Reference Designator	Value	Part #	Manufacturer
L	1.0 nH	0402CC-1N0XJL	Coilcraft
C	0.4 pF	0603N0R4BW251	Passive Plus Inc.

11.0 Device Package Information

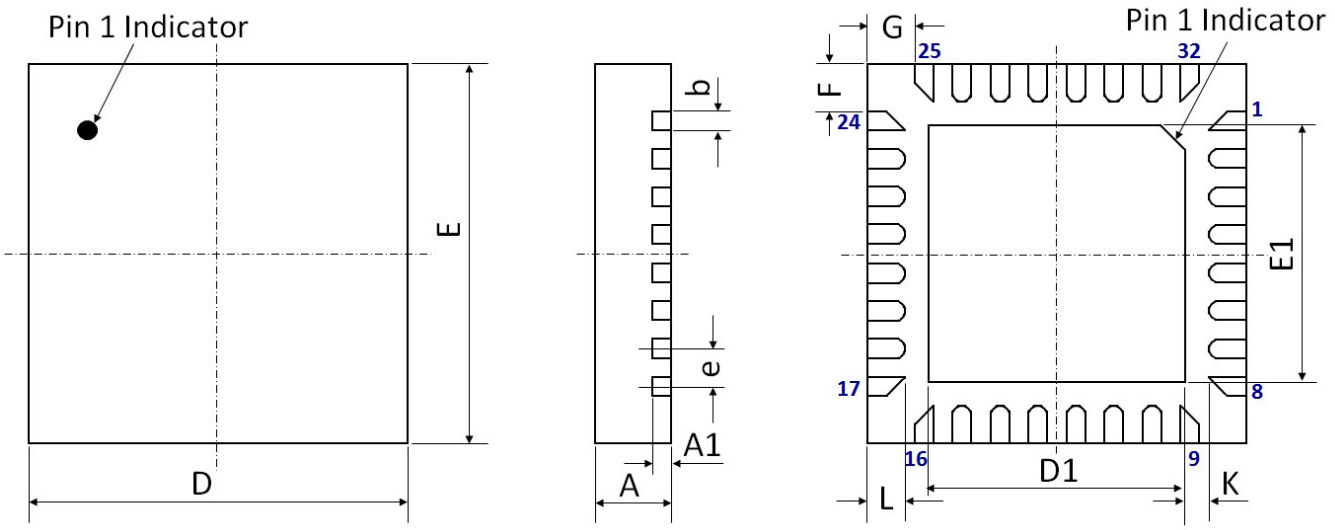


Figure 6 Device Package Drawing
(All dimensions are in mm)

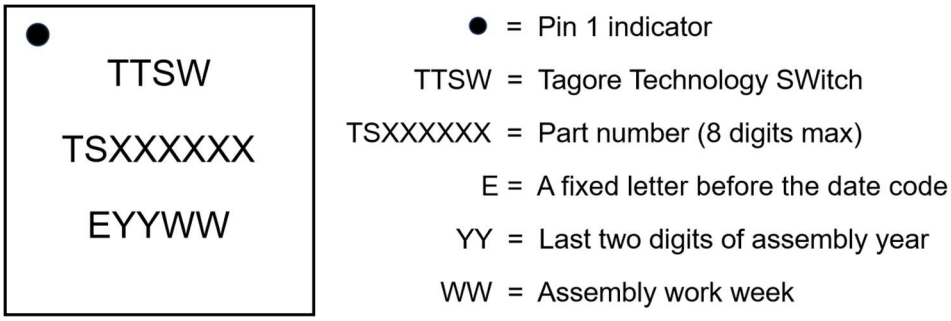
Table 6 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.80	±0.05	E	4.00 BSC	±0.05
A1	0.203	±0.02	E1	2.70	±0.05
b	0.20	+0.05/-0.07	F	0.50	±0.05
D	4.00 BSC	±0.05	G	0.50	±0.05
D1	2.70	±0.05	L	0.40	±0.05
e	0.40 BSC	±0.05	K	0.25	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

Top-marking specification:



12.0 PCB Land Design

Guidelines:
[1] 4-layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 4(X)×4(Y)=16.

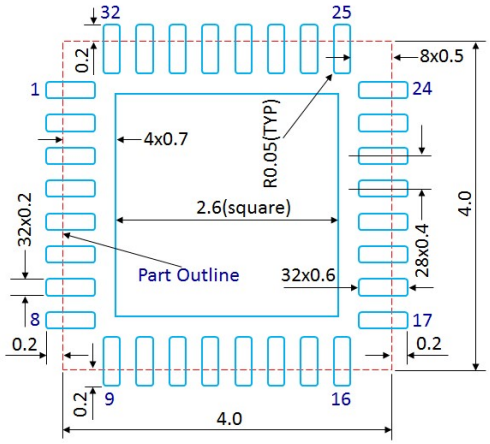


Figure 7 PCB Land Pattern
(Dimensions are in mm)

Non-Solder Mask Defined (Preferred)

Solder Mask Defined

Figure 8 Solder Mask Pattern
(Dimensions are in mm)

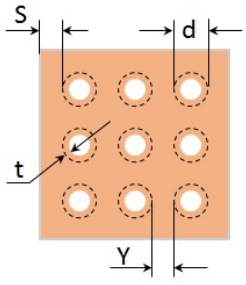


Figure 9 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

13.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125μm.

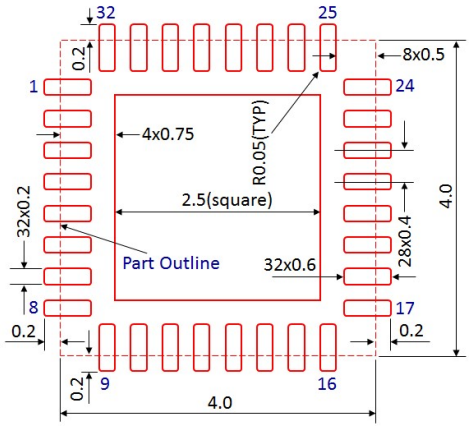


Figure 10 Stencil Openings
(Dimensions are in mm)

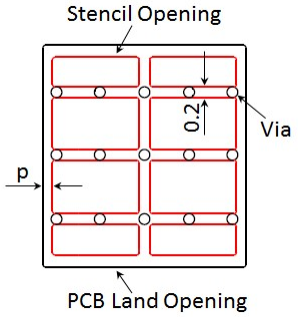


Figure 11 Stencil Openings Shall Not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

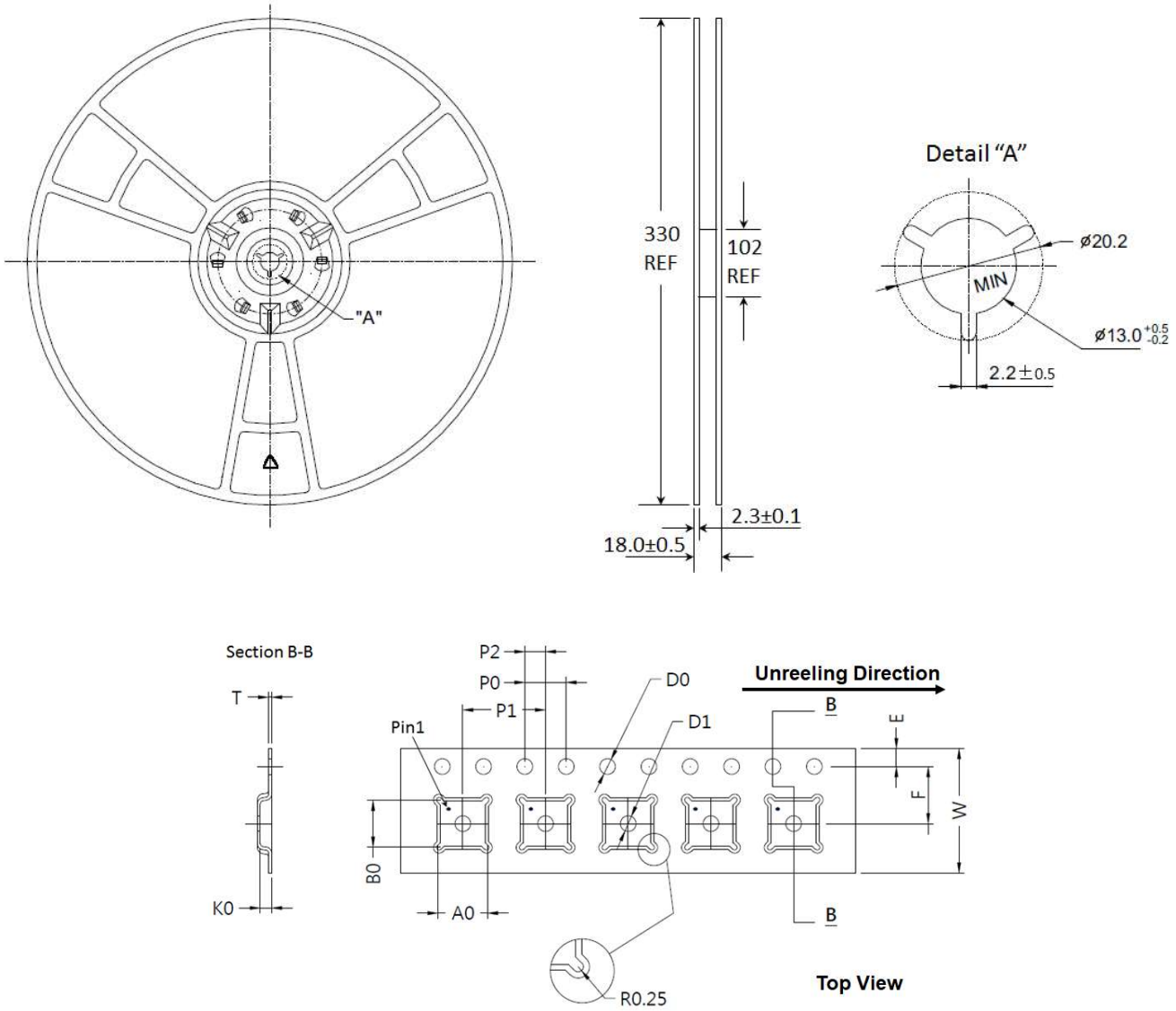


Figure 12 Tape and Reel Drawing

Table 7 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	4.35	±0.10	K0	1.10	±0.10
B0	4.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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