TSL8329M: Dual channel 2.0 – 4.2 GHz 20-Watt Receiver Front End

1.0 Features

Integrated dual-channel RF front end
2-stage LNA and GaN SPDT switch On-chip bias and matching Single-supply operation

- Gain @ 3.6 GHz: 32 dB (High Gain mode)
  @ 3.6 GHz: 13 dB (Low Gain mode)
- NF @ 3.6 GHz: 1.0 dB (High Gain mode)
  @ 3.6 GHz: 0.9 dB (Low Gain mode)
- OP1dB@ 3.6 GHz: 20 dBm (High Gain mode)
  @ 3.6 GHz: 10.5 dBm (Low Gain mode)
- Operating frequency: 2.0 to 4.2 GHz
- High Isolation**:** RXOUT-CHA & RXOUT-CHB: 40 dB typical
- TERM-CHA and TERM-CHB: 55 dB typical
- Insertion loss @ 3600 MHz: 0.45 dB (TX mode)
- High power handling at TCASE = 105°C Full lifetime
- LTE average power (9 dB PAR): 43 dBm
- High OIP3 (high gain mode): 35 dBm typical
- High gain mode current: 90 mA typical at 5 V
- Low gain mode current: 45 mA typical at 5 V
- Power-down mode current: 5 mA typical at 5 V Positive logic control
- 6 mm × 6 mm, 40-Pin QFN

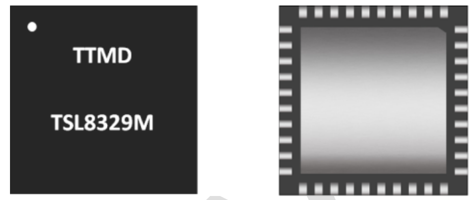


Figure 1.1 Device Image
(40 Pin 6×6×0.85 mm QFN Package)

2.0 Applications

- 4G/5G Infrastructure Radios
- Small Cells and Cellular Repeaters
- Phase Array Radar
- SDARS

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TSL8329M is a dual-channel, integrated RF, front-end, multichip module designed for different applications. The device operates from 2.0 GHz to 4.2 GHz. The TSL8329M is configured in dual channels with a cascading, two-stage, LNA and a high GaN based SPDT switch.
In high gain mode, the cascaded two-stage LNA and switch offer a low noise figure of 1 dB and a high gain of 32 dB at 3.6 GHz with an output third-order intercept point (OIP3) of 35 dBm (typical) at high gain mode. In low gain mode, one stage of the two-stage LNA is in bypass, providing 13 dB of gain at a lower current of 45 mA. In power-down mode, the LNAs are turned off and the device draws 5 mA.
In transmit operation, when RF inputs are connected to a termination pin (TERM-CHA or TERM-CHB), the switch provides low insertion loss of 0.45 dB at 3.6 GHz and handles long-term evolution (LTE) average power (9 dB peak to average ratio (PAR)) of 43 dBm for full lifetime operation.

The device comes in an RoHS compliant, compact, 6 mm × 6 mm, 40-Pin QFN.

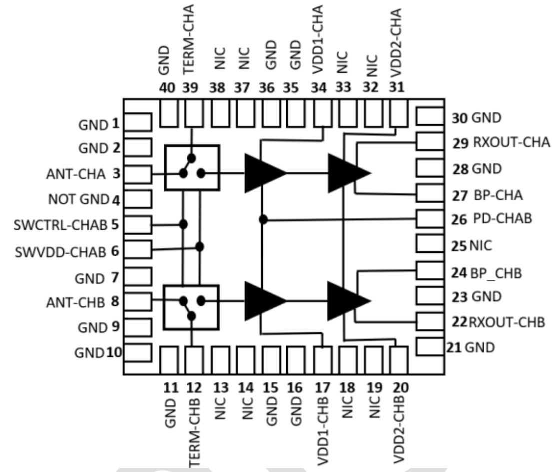


Figure 3.1 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 4.1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TSL8329M	40 Pin 6×6×0.85 mm QFN	Tape & Reel	3000	13” (330 mm)	18 mm	TSL8329MMTRPBF
Tuned Evaluation Board, 3300 – 4000 MHz						TSL8329M-EVB-A
Tuned Evaluation Board, 2900 – 3300 MHz						TSL8329M-EVB-B
Tuned Evaluation Board, 2000 – 4000 MHz						TSL8329M-EVB-C

5.0 Pin Description

Table 5.1 Pin Definition

Pin Number	Pin Name	Description
1, 2, 7, 9 to 11, 15, 16, 21, 23, 28, 30, 35, 36, 40	GND	Ground
4	NOT GND	Internally used. Don't make it GND. Left unconnected.
3	ANT-CHA	RF Input to Channel A. The ANT-CHA pin is ac-coupled to 0 V and matched to 50 Ω. Matching and a dc blocking capacitor are not required.
5	SWCTRL-CHAB	Control Voltage for Switches on Channel A and Channel B.
6	SWVDD-CHAB	Supply Voltage for Switches on Channel A and Channel B.
8	ANT-CHB	RF Input to Channel B. The ANT-CHB pin is ac-coupled to 0 V and matched to 50 Ω. Matching and a dc blocking capacitor are not required.
12	TERM-CHB	Termination Output for Channel B. The TERM-CHB pin is the transmitter path for Channel B. The TERM-CHB pin is ac-coupled to 0 V and matched to 50 Ω. No matching and dc blocking capacitor required.
13, 14, 18, 19, 25, 32, 33, 37, 38	NIC	Not Internally Connected. It is recommended to connect NIC to the RF ground of the PCB.
17	VDD1-CHB	Vdd1 supplied through an external choke inductor
20	VDD2-CHB	Vdd2 supplied through an external choke inductor
22	RXOUT-CHB	Receiver Output. The RXOUT -CHB pin is the receiver path for Channel B. The RXOUT -CHB pin is ac matched to 50 Ω. No matching component is required. A dc blocking capacitor is required.
24	BP-CHB	Bypass Second Stage LNA of Channel B.
26	PD-CHAB	Power-Down All Stages of LNA for Channel A and Channel B.
27	BP-CHA	Bypass Second Stage LNA of Channel A.
29	RXOUT-CHA	Receiver Output. The RXOUT-CHA pin is the receiver path for Channel A. The RXOUT-CHA pin is ac matched to 50 Ω. No matching component is required. A dc blocking capacitor is required.
34	VDD1-CHA	Vdd1 supplied through an external choke inductor
31	VDD2-CHA	Vdd2 supplied through an external choke inductor
39	TERM-CHA	Termination Output for Channel A. The TERM-CHA pin is the transmitter path for Channel A. The TERM-CHA pin is ac-coupled to 0 V and matched to 50 Ω. No matching and dc blocking capacitor required
Package Base	Paddle/Slug	DC and RF Ground. Also provides thermal relief. Multiple vias are recommended

Note: [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heat sinking required.

6.0 Absolute Maximum Rating

Table 6.1 Absolute Maximum Rating @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Supply voltage, VDD1-CHA, VDD1-CHB, VDD2-CHA, VDD2-CHB and SWVDD-CHAB	V_{dd}	+5.5	V
RF input power Transmit Input Power (AVG, LTE with 8dB PAR,) Receive Input Power (LTE Peak, 8 dB PAR)	RF_{IN}	43 25	dBm dBm
Digital Control Input Voltage SWCTRL-CHAB, BP-CHA, BP-CHB, and PD-CHAB		1.8 to 5.5	V
Digital Control Input Current SWCTRL-CHAB, BP-CHA, BP-CHB, and PD-CHAB		0.2	mA
Storage Temperature Range	T_{st}	-55 to +150	°C
Operating Temperature Range	T_{op}	-40 to +105	°C
Maximum Junction Temperature	T_J	170	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	15.0	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Recommended DC Operating Conditions

Table 7.1 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltages	VDD1-CHA, VDD1-CHB		+5.0		V
	VDD2-CHA, VDD2-CHB		+5.0		
Drain Bias Currents	$I_{DQ1,}$ Set by external drain feed		45		mA
	$I_{DQ2,}$ Set by external drain feed		90		
Switch Supply	SWVDD-CHAB		+5		V
Switch Control Voltages	SWCTRL-CHAB, BP-CHA, BP-CHB, PD-CHAB	0		+5.5	V
RF Input Power At ANT-CHA, ANT-CHB	PD-CHAB = 5 V, BP-CHA = BP-CHB = 0 V. 8 dB PAR LTE full lifetime average			43	dBm
	PD-CHAB = 0 V, BP-CHA = BP-CHB = 0 V, 8 dB PAR LTE full lifetime average			31	dBm
	PD-CHAB = 0 V, BP-CHA = BP-CHB = 5 ,8 dB PAR LTE full lifetime average,			43	dBm
DIGITAL INPUT SWCTRL-CHAB, PD-CHAB Low (VIL) High (VIH) BP-CHA, BP-CHB Low (VIL) High (VIH)		0 0.9 0 0.9		0.2 Vdd 0.2 Vdd	V
DIGITAL INPUT CURRENTS SWCTRL-CHAB PD-CHAB BP-CHA, BP-CHB	SWCTRL-CHAB, PD-CHAB, BP-CHA, BP-CHB = 5 V per channel			<7.5 200 100	µA
Switch control max current				7.5	µA
Operating Temperature Range	T_{op}	-40	+25	+105	°C

8.0 RF Electrical Specifications for EVBs

VDD1-CHA, VDD1-CHB, VDD2-CHA, VDD2-CHB, and SWVDD-CHAB = 5 V, SWCTRL-CHAB = 0 V or SWVDD-CHAB, BP-CHA = VDD1-CHA or 0 V, BP-CHB = VDD1-CHB or 0 V, PD-CHAB = 0 V or VDD1-CHA, TCASE = 25°C, and 50 Ω system, unless otherwise noted.

Table 8.1 3300 – 4000 MHz EVB A

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Operational frequency Range		3.3 G	3.6 G	4.0 G	Hz
Gain	LNAs on Bypass off (High gain)		32		dB
	LNA1 on Bypass on (Low gain)		13		dB
Noise Figure (De-embedded)	LNAs on Bypass off (High gain)		1		dB
	LNA1 on Bypass on (Low gain)		0.9		dB
EVB Noise Figure	LNAs on Bypass off (High gain)		1.4		dB
	LNA1 on Bypass on (Low gain)		1.3		dB
Input Return Loss	LNAs on Bypass off (High gain)		10		dB
	LNA1 on Bypass on (Low gain)		5		dB
Output Return Loss	LNAs on Bypass off (High gain)		11		dB
	LNA1 on Bypass on (Low gain)		9		dBm
OP1dB	LNAs on Bypass off (High gain)		20		dBm
	LNA1 on Bypass on (Low gain)		10.5		dBm
OIP3	LNAs on Bypass off (High gain)0 dBm per tone, Tone Spacing 1 MHz		35		dBm
	LNA1 on Bypass on (Low gain) -2 dBm per tone, Tone Spacing 1 MHz		18		dBm
Current, Id	LNAs on Bypass off (High gain)		90		mA
	LNA1 on Bypass on (Low gain)		45		
	PD mode ON (Both LNAs OFF)		5		
Insertion Loss	Transmit operation at 3.6 GHz		0.45		dB
Channel to Channel Isolation Between RXOUT -CHA & RXOUT -CHB	At 3.6 GHz Receive operation		40		dB
Between TERM-CHA AND TERM-CHB	Transmit operation		55		dB
SWITCH ISOLATION ANT-CHA to TERM-CHA and ANT-CHB to TERM-CHB	Transmit operation, PD-CHAB=0 V		25		dB
SWITCHING CHARACTERISTICS (tON, tOFF)	50% control voltage to 90%, 10% of RXOUT -CHA or RXOUT -CHB in receive operation		400		ns
	50% control voltage to 90%, 10% of TERM-CHA or TERM-CHB in transmit operation		400		

Table 8.2 2900 – 33000MHz EVB B

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Operational frequency Range		2.9 G	3.1 G	3.3 G	Hz
Gain	LNAs on Bypass off (High gain)		38-35		dB
	LNA1 on Bypass on (Low gain)		15-13.5		dB
Noise Figure (De-embedded)	LNAs on Bypass off (High gain)		0.9-1		dB
	LNA1 on Bypass on (Low gain)		0.9-1		dB
EVB Noise Figure	LNAs on Bypass off (High gain)		1.4-1.3		dB
	LNA1 on Bypass on (Low gain)		1.4-1.3		dB
Input Return Loss	LNAs on Bypass off (High gain)		9-9.5		dB
	LNA1 on Bypass on (Low gain)		9-10		dB
Output Return Loss	LNAs on Bypass off (High gain)		11-17		dB
	LNA1 on Bypass on (Low gain)		4-5.4		dBm
OP1dB	LNAs on Bypass off (High gain)		17-18		dBm
	LNA1 on Bypass on (Low gain)		10-11		dBm
OIP3	LNAs on Bypass off (High gain)0 dBm per tone, Tone Spacing 1 MHz		32.5-30		dBm
	LNA1 on Bypass on (Low gain) -2 dBm per tone, Tone Spacing 1 MHz		25-20		dBm
Current, Id	LNAs on Bypass off (High gain)		90		mA
	LNA1 on Bypass on (Low gain)		45		
	PD mode ON (Both LNAs OFF)		5		
Insertion Loss	Transmit operation at 3.1 GHz		0.45		dB
Channel to Channel Isolation Between RXOUT -CHA & RXOUT -CHB	At 3.1 GHz Receive operation		35		dB
Between TERM-CHA AND TERM-CHB	Transmit operation		55		dB
SWITCH ISOLATION ANT-CHA to TERM-CHA and ANT-CHB to TERM-CHB	Transmit operation, PD-CHAB = 0 V		30		dB
SWITCHING CHARACTERISTICS (tON, tOFF)	50% control voltage to 90%, 10% of RXOUT -CHA or RXOUT -CHB in receive operation		400		ns
	50% control voltage to 90%, 10% of TERM-CHA or TERM-CHB in transmit operation		400		

Table 8.3 2000 – 4000MHz EVB C

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Operational frequency Range		2.0 G	3.0 G	4.0 G	Hz
Gain	LNAs on Bypass off (High gain)		37-29		dB
	LNA1 on Bypass on (Low gain)		18-12		dB
Noise Figure (De-embedded)	LNAs on Bypass off (High gain)		0.7-1.2		dB
	LNA1 on Bypass on (Low gain)		0.7-1.2		dB
EVB Noise Figure	LNAs on Bypass off (High gain)		1.1-1.6		dB
	LNA1 on Bypass on (Low gain)		1.1-1.6		dB
Input Return Loss	LNAs on Bypass off (High gain)		7.3-3.3		dB
	LNA1 on Bypass on (Low gain)		4.2-7.3		dB
Output Return Loss	LNAs on Bypass off (High gain)		4-17		dB
	LNA1 on Bypass on (Low gain)		3-24		dBm
OP1dB	LNAs on Bypass off (High gain)		18.5-20.5		dBm
	LNA1 on Bypass on (Low gain)		7-12		dBm
OIP3	LNAs on Bypass off (High gain)0 dBm per tone, Tone Spacing 1 MHz		31-35		dBm
	LNA1 on Bypass on (Low gain) -2 dBm per tone, Tone Spacing 1 MHz		17-21		dBm
Current, Id	LNAs on Bypass off (High gain)		90		mA
	LNA1 on Bypass on (Low gain)		45		
	PD mode ON (Both LNAs OFF)		5		
Insertion Loss	Transmit operation at 3.0 GHz		0.45		dB
Channel to Channel Isolation Between RXOUT -CHA & RXOUT -CHB	At 3.0 GHz Receive operation		35		dB
Between TERM-CHA AND TERM-CHB	Transmit operation		55		dB
SWITCH ISOLATION ANT-CHA to TERM-CHA and ANT-CHB to TERM-CHB	Transmit operation, PD-CHAB = 0 V		30		dB
SWITCHING CHARACTERISTICS (tON, tOFF)	50% control voltage to 90%, 10% of RXOUT -CHA or RXOUT -CHB in receive operation		400		ns
	50% control voltage to 90%, 10% of TERM-CHA or TERM-CHB in transmit operation		400		

9.0 Typical performance characteristics

9.1 Receive Operation, LOW GAIN Mode 3.3-4.0 GHz tuned EVB -40ºC,25ºC,85ºC,105 ºC

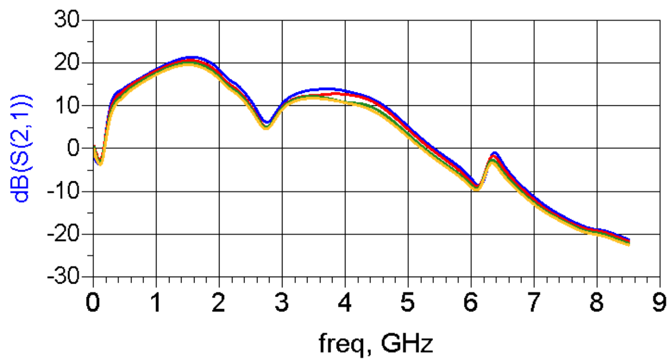


Figure 9.1.1 S21 (Gain) vs Freq

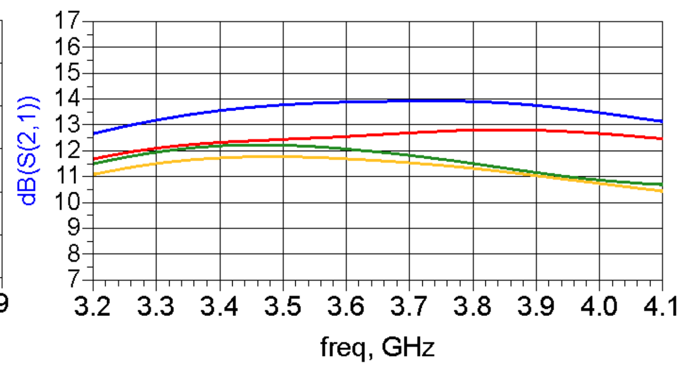


Figure 9.1.2 S21 (Gain) vs Freq

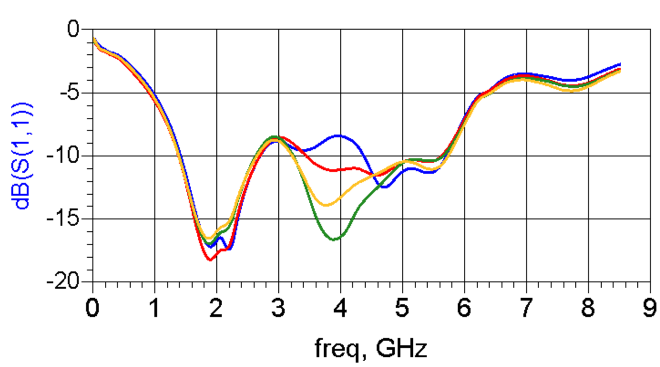


Figure 9.1.3 S11 (IRL) vs Freq

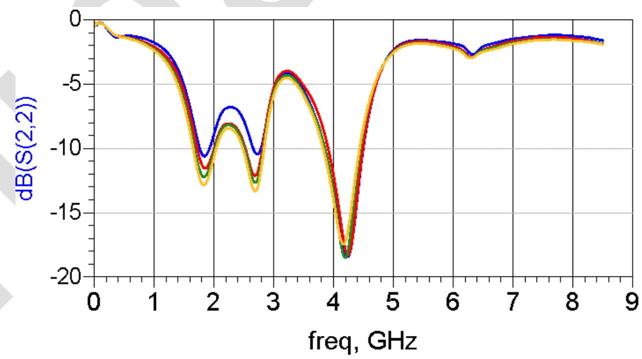


Figure 9.1.4 S22(ORL) vs Freq

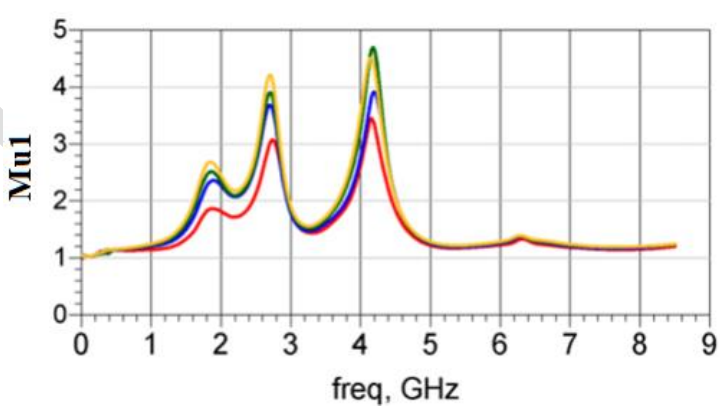


Figure 9.1.5 Mu1 vs Freq

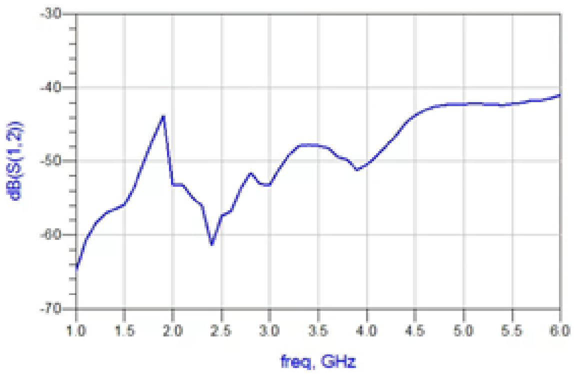


Figure 9.1.6 Channel to channel isolation vs Freq

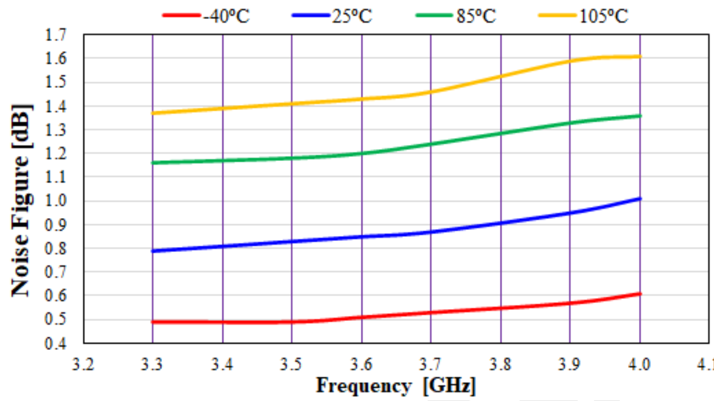


Figure 9.1.7 NF(De-embedded) vs Freq

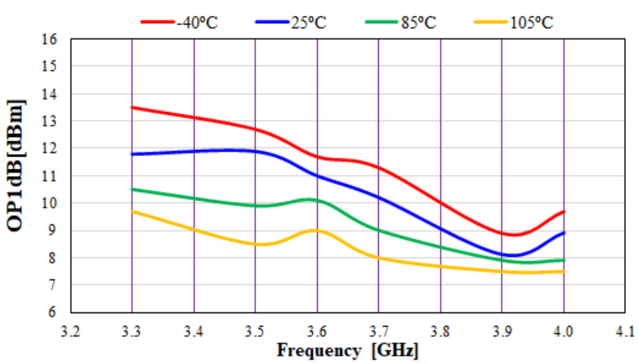


Figure 9.1.8 OP1dBm vs Freq

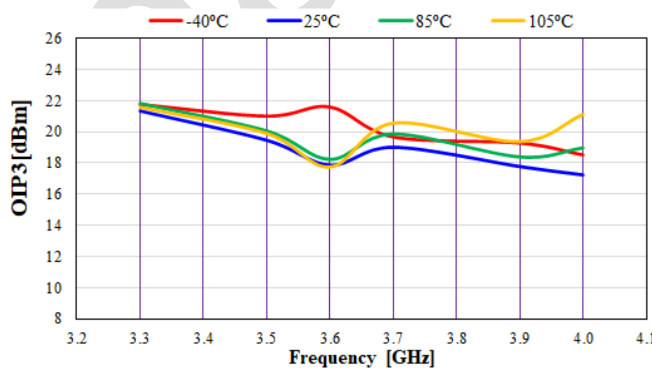


Figure 9.1.9 OIP3dBm vs Freq

9.2 Receive Operation, HIGH GAIN Mode 3.3-4.0 GHz tuned EVB -40°C,25°C,85°C,105 °C

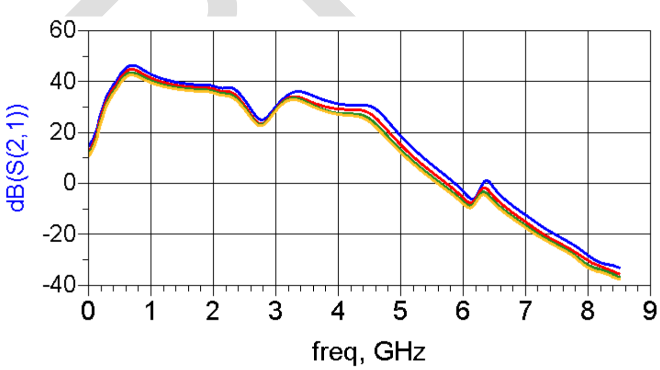


Figure 9.2.1 S21 (Gain) vs Freq

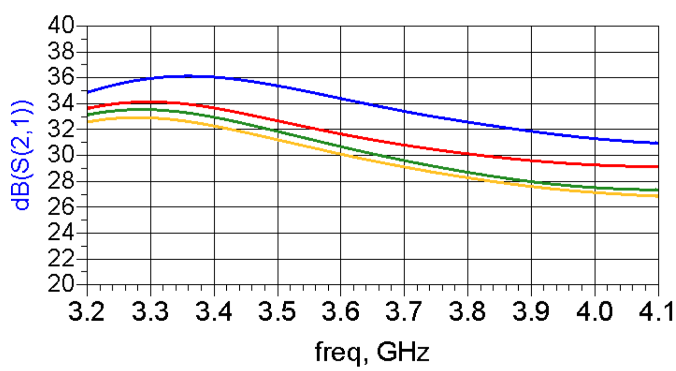


Figure 9.2.2 S21 (Gain) vs Freq

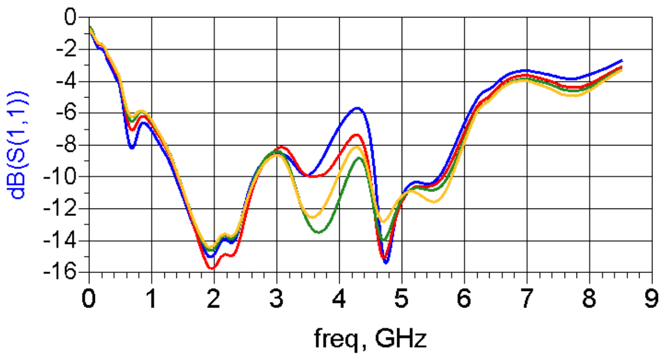


Figure 9.2.3 S11 (IRL) vs Freq

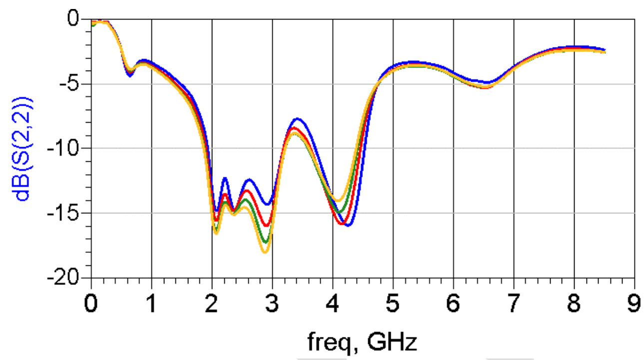


Figure 9.2.4 S22(ORL) vs Freq

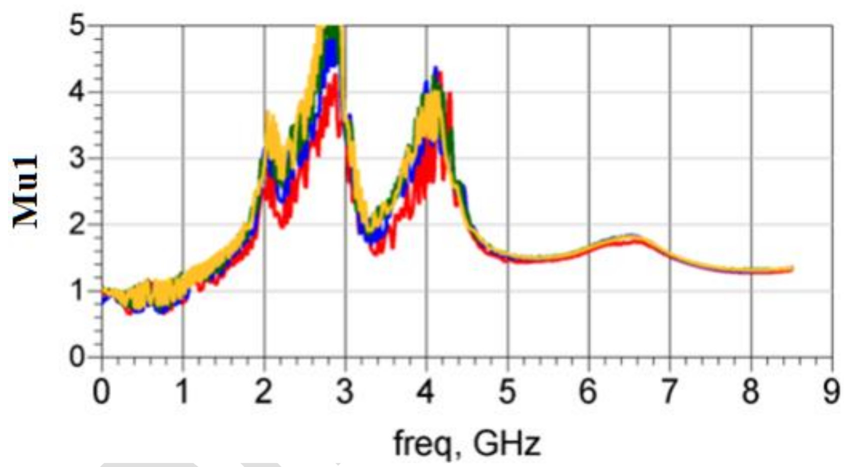


Figure 9.2.5 Mu1 vs Freq

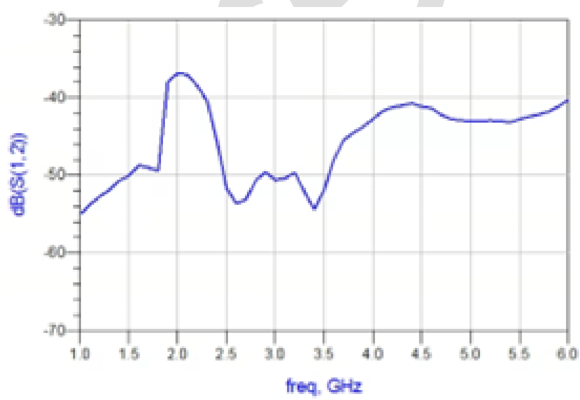


Figure 9.2.6 Channel to channel isolation vs Freq

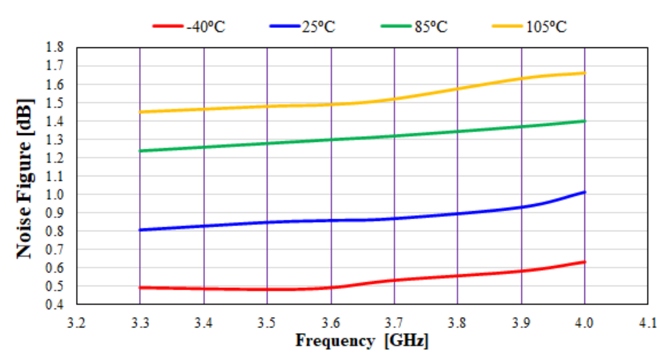


Figure 9.2.7 NF(De-embedded) vs Freq

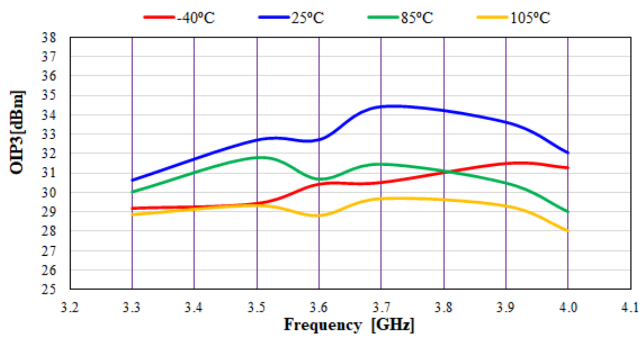


Figure 9.2.7 OIP3dBm vs Freq

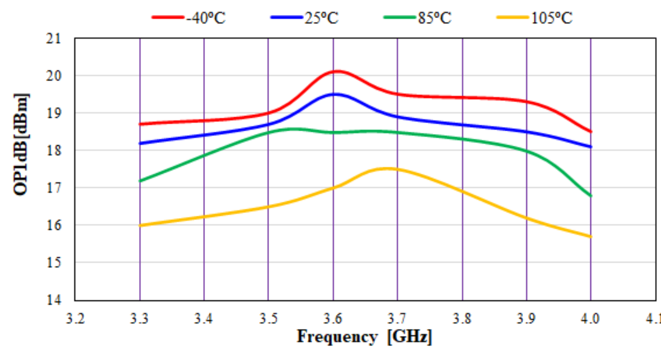


Figure 9.2.8 OP1dBm vs Freq

9.3 Transmit Operation 3.3-4.0GHz tuned EVB -40°C,25°C,85°C,105 °C

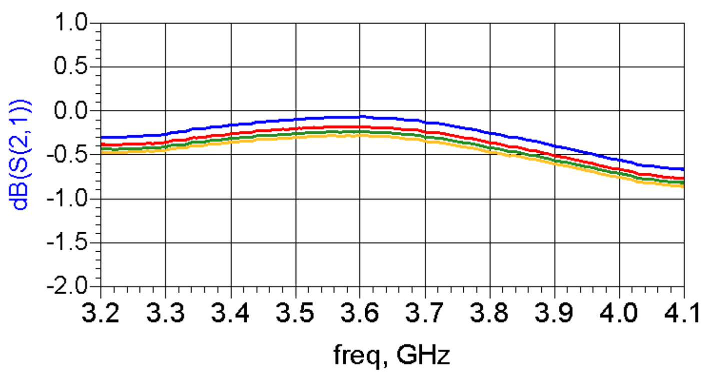


Figure 9.3.1 IL vs Freq

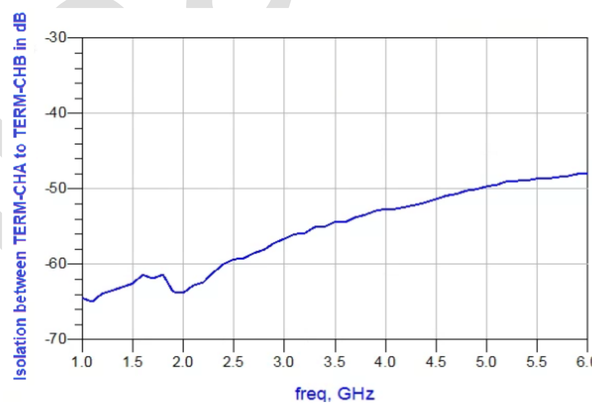


Figure 9.3.2 TERM-CHA and TERM-CHB isolation

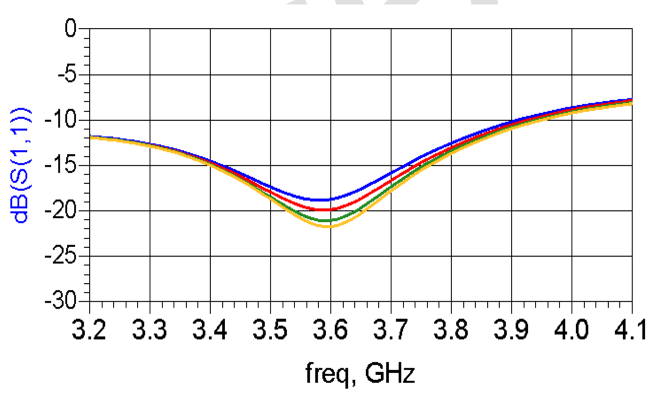


Figure 9.3.3 Input return loss vs Freq

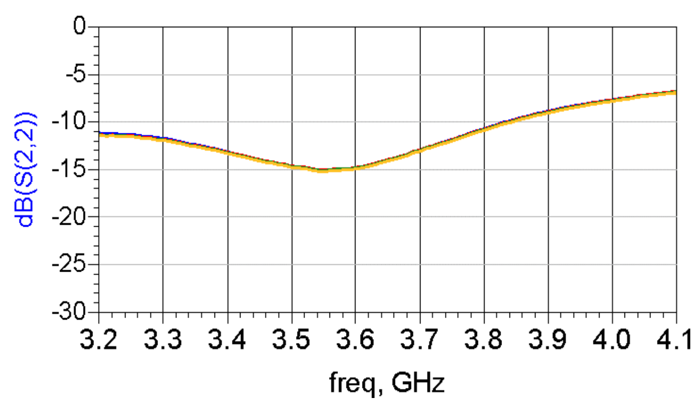


Figure 9.3.4 Output return loss vs Freq

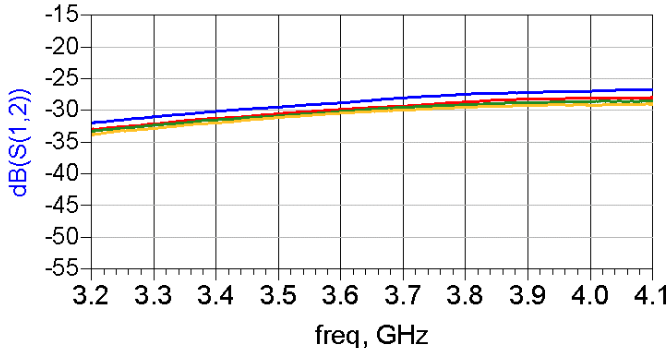


Figure 9.3.5 ANT to TERM isolation vs Freq, LNA on

10.0 Evaluation Boards

10.1 3300- 4000 MHz EVB A

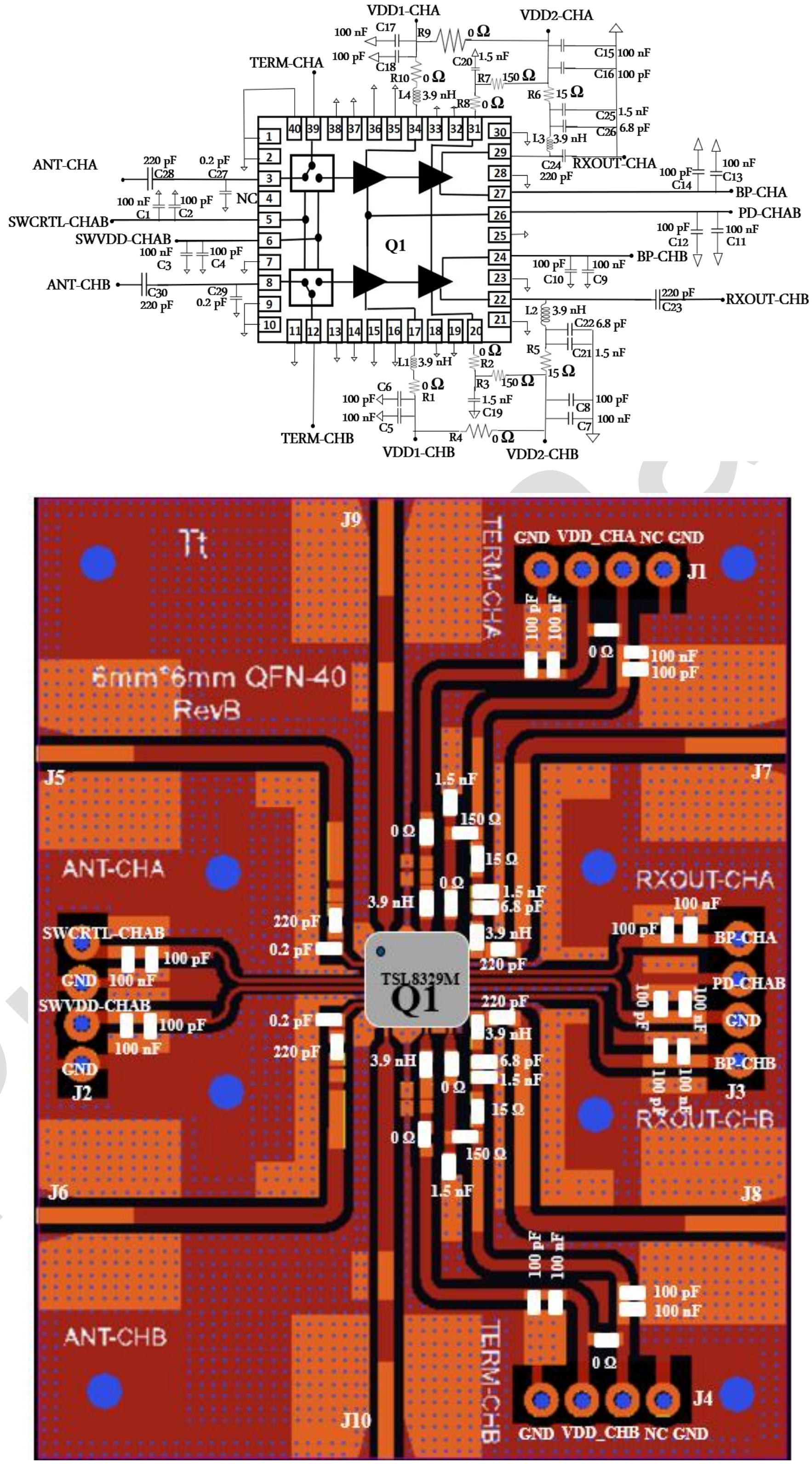


Figure 10.1 Schematic and Layout of the 3300 – 4000 MHz EVB A

Table 10.1 BOM of the 3300 – 4000 MHz EVB A

Component ID	Value	Manufacturer	Recommended Part Number	Qty
R1, R2, R4, R8, R9, R10	0 Ω	Panasonic	ERJ-2GE0R00X	6
R3, R7	150 Ω	Panasonic	ERJ-2RHD1500X	2
R5, R6	15 Ω	Panasonic	ERJ-H2RD15R0X	2
L1, L2, L3, L4	3.9 nH	Coil craft/ Wurth Electronics	0402HP-3N9XGRW/ 744916039	4
C22, C26	6.8 pF	Murata	GJM1555C1H6R8BB01D	2
C19, C20, C21, C25	1.5 nF	Murata	04025C152JAT2A	4
C23, C24, C28, C30	220 pF	Kemet	C0402C221K5GACAUTO	4
C27, C29	0.2 pF	Murata	GJM1555C1HR20BB01D	2
C2, C4, C6, C8, C10, C12, C14, C16, C18	100 pF	AVX	04025A101JAT4A	9
C1, C3, C5, C7, C9, C11, C13, C15, C17	100 nF	TDK	C1005X7R1H104K050BE	9
Q1	GaAs LNA+ GaN Switch	TagoreTech	TSL8329M	1
PCB	Rogers RO4350B, 20 mils, 1 oz copper			1

10.2 2900- 3300 MHz EVB B

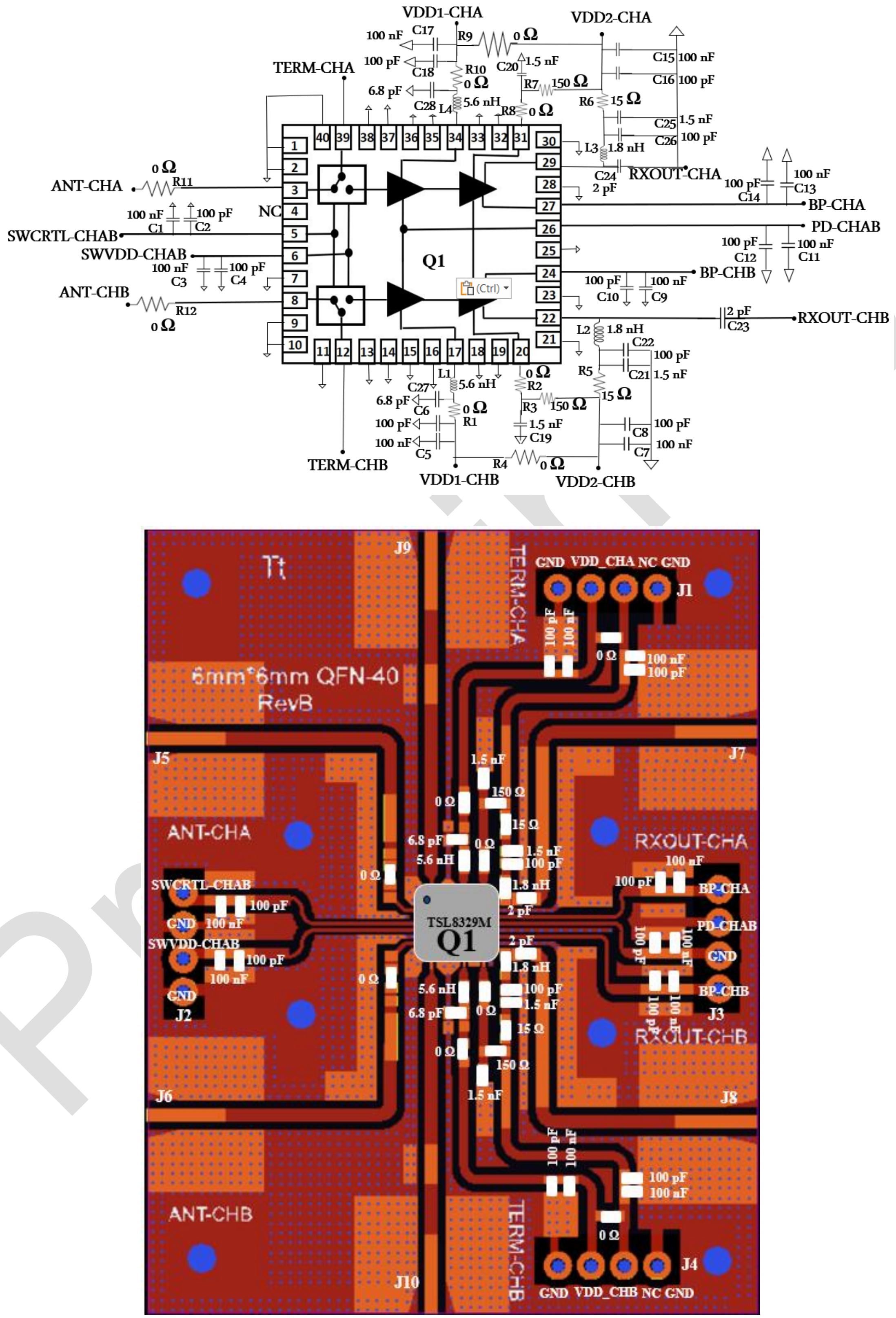


Figure 10.2 Schematic and Layout of the 2900 – 3300 MHz EVB B

Table 10.2 BOM of the 2900 – 3300 MHz EVB B

Component ID	Value	Manufacturer	Recommended Part Number	Qty
R1, R2, R4, R8, R9, R10, R11, R12	0 Ω	Panasonic	ERJ-2GE0R00X	6
R3, R7	150 Ω	Panasonic	ERJ-2RHD1500X	2
R5, R6	15 Ω	Panasonic	ERJ-H2RD15R0X	2
L2, L3	1.8 nH	Coil craft/ Wurth Electronics	0603HP-1N8XJLW/ 744761018A	2
L1, L4	5.6 nH	Coil craft/ Wurth Electronics	0402HP-5N6XGRW/ 744916056	2
C27, C28	6.8 pF	Murata	GJM1555C1H6R8BB01D	2
C19, C20, C21, C25	1.5 nF	Murata	04025C152JAT2A	4
C23, C24	2 pF	Murata	GJM1555C1H2R0BB01D	2
C2, C4, C6, C8, C10, C12, C14, C16, C18, C22, C26	100 pF	AVX	04025A101JAT4A	9
C1, C3, C5, C7, C9, C11, C13, C15, C17	100 nF	TDK	C1005X7R1H104K050BE	9
Q1	GaAs LNA+ GaN Switch	TagoreTech	TSL8329M	1
PCB	Rogers RO4350B, 20 mils, 1 oz copper			1

10.3 2000- 4000 MHz EVB C

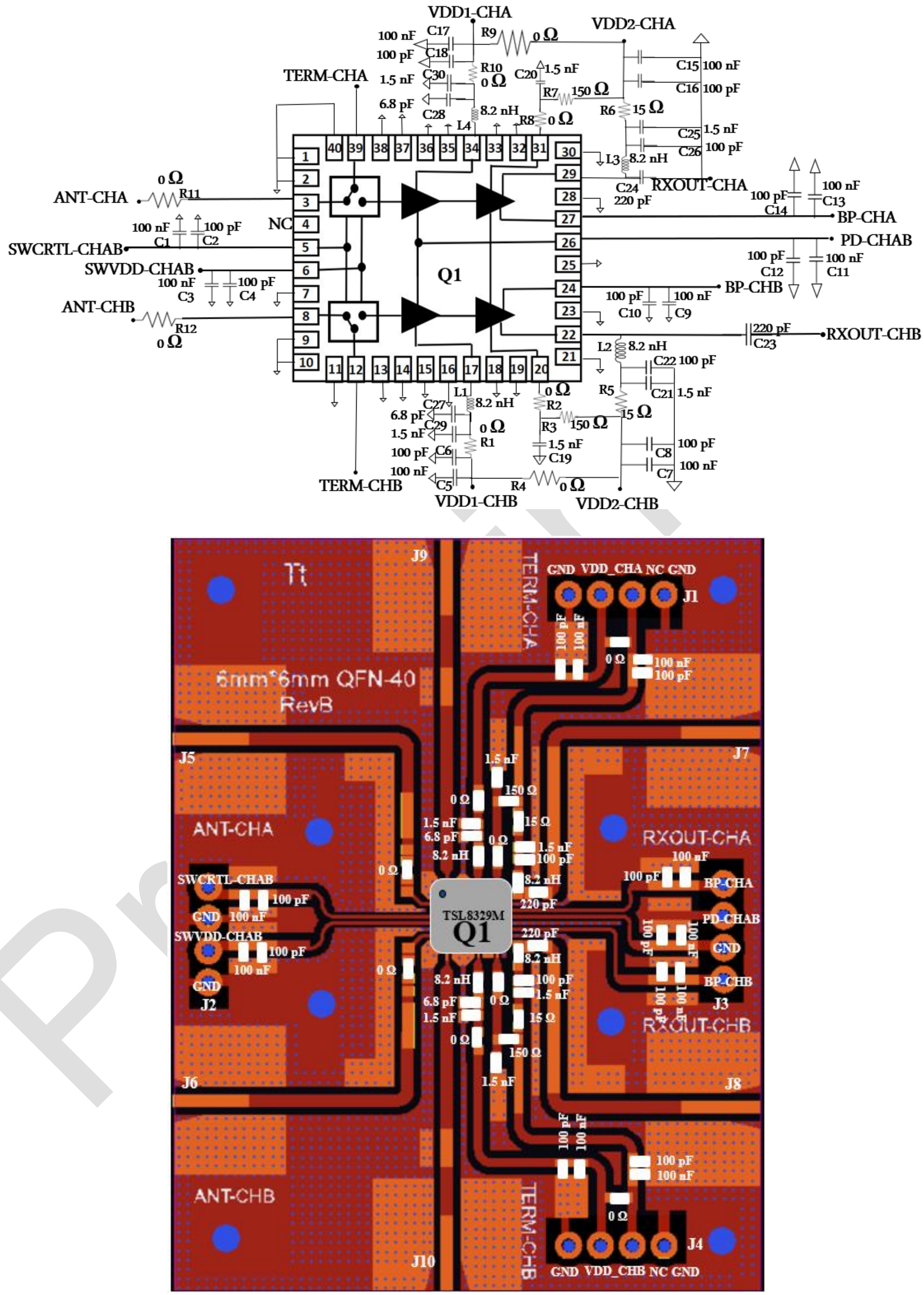


Figure 10.3 Schematic and Layout of the 2000 – 4000 MHz EVB C

Table 10.3 BOM of the 2000 – 4000 MHz EVB C

Component ID	Value	Manufacturer	Recommended Part Number	Qty
R1, R2, R4, R8, R9, R10, R11, R12	0 Ω	Panasonic	ERJ-2GE0R00X	8
R3, R7	150 Ω	Panasonic	ERJ-2RHD1500X	2
R5, R6	15 Ω	Panasonic	ERJ-H2RD15R0X	2
L1, L2, L3, L4	8.2 nH	Coil craft/ Wurth Electronics	0402HP-8N2XGRW/ 744916082	2
C27, C28	6.8 pF	Murata	GJM1555C1H6R8BB01D	2
C19, C20, C21, C25, C29, C30	1.5 nF	Murata	04025C152JAT2A	6
C23, C24	220 pF	Murata	C0402C221K5GACAUTO	2
C2, C4, C6, C8, C10, C12, C14, C16, C18, C22, C26	100 pF	AVX	04025A101JAT4A	11
C1, C3, C5, C7, C9, C11, C13, C15, C17	100 nF	TDK	C1005X7R1H104K050BE	9
Q1	GaAs LNA+ GaN Switch	TagoreTech	TSL8329M	1
PCB	Rogers RO4350B, 20 mils, 1 oz copper			1

10.4 EVB TEST Details

Table 10.4 RF-DC Connector details

Connector Names & type	Voltage names	Description
J1- DC header	VDD-CHA	Supply LNA on Channel A
J2- DC header	SWVDD-CHAB & SWCRTL-CHAB	Supply switches on Channel A and Channel B Control switches on Channel A and Channel B
J3- DC header	BP-CHA, BP-CHB PD-CHAB	Bypass LNA Stage 2 on Channel A Bypass LNA Stage 2 on Channel B Power down all LNA stages on Channel A and B
J4- DC header	VDD-CHB	Supply LNA on Channel B
J5- RF connector	ANT-CHA	Antenna input to Channel A
J6- RF connector	ANT-CHB	Antenna input to Channel B
J7- RF connector	RXOUT-CHA	Receiver output from Channel A
J8- RF connector	RXOUT-CHB	Receiver output from Channel A
J9- RF connector	TERM-CHA	Termination output from Channel A
J10- RF connector	TERM-CHB	Termination output from Channel B

All the connectors and headers' names are given in the EVB layout figure [Figure no 10.2/10.4]

Table 10.5 Truth Table: Switch control

SWCTRL-CHAB	Signal Path Select	
	Transmit Operation	Receive Operation
Low High	Off On	On Off

Table 10.6 Truth Table: Receive Operation

Receive Operation	PD-CHAB	BP-CHA BP-CHB	Signal Path
High Gain Mode	Low	Low	ANT-CHA to RXOUT-CHA, ANT-CHB to RXOUT-CHB
Low Gain Mode	Low	High	
Power-Down High Isolation Mode	High	Low	
Power-Down Low Isolation Mode	High	High	

10.7.1 TEST PROCEDURE

Biasing sequence

To bias up the TSL8329M-EVB-A for Channel A, perform the following steps:

1. Ground the GND or GND1 test point.
2. Bias up SWVDD-CHAB=5 V test points.
3. Bias up the SWCTRL-CHAB test point.
4. Bias up the VDD-CHA test point.
5. Bias up the BP-CHA test points.
6. Bias up the PD-CHAB test point.
7. Apply an RF input signal.

The TSL8329-EVB-A is shipped fully assembled and tested. Figure 10.7.1 provides a basic test setup diagram to evaluate the s-parameters in RX mode to get Channel-A performance (receive gain, transmit insertion loss and isolation, RF input and output return losses) using a network analyzer. Perform the following steps to complete the test setup and verify the operation of the TSL8329-EVB-A:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the VDD-CHA and SWVDD-CHAB test points to the voltage output terminal of the 5 V supply that sources a current of approximately 90 mA in receive operation for high gain mode or 5 mA for power-down mode.
3. Connect the BP-CHA, BP-CHB, PD-CHAB, and SWCTRL-CHAB test points to the ground terminal of the power supply for high gain receive operation. The TSL8329-EVB-A can be configured in different modes by connecting the control test points to 5 V or ground, as shown in Table 10.3 and Table 10.4.
4. Connect a calibrated network analyzer to the ANT-CHA, TERM-CHA, and RXOUT-CHA SMA connectors. Sweep frequency from 1 GHz to 6 GHz and set power to −25 dBm.
5. Connect 50 Ω loads to the ANT-CHB, TERM-CHB, and RXOUT-CHB SMA connectors.
6. The TSL8329-EVB-A is expected to have a high and low receive gain of 32 dB and 13 dB respectively, at 3.6 GHz. See the expected results in Figure 9.2.1 to Figure 9.1.1.

Additional test equipment is needed to fully evaluate the device’s functions and performance.

For noise figure evaluation, use either a noise figure analyzer or a spectrum analyzer with noise option. The use of a low excess noise ratio (ENR) noise source is recommended.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is recommended.

For power compression and power handling evaluations, use a two-channel power meter and a signal generator. A power amplifier with great enough power is recommended at the input. Test accessories such as couplers and attenuators must have enough power handling.

The TSL8329-EVB-A comes with a support plate attached to the bottom side. To ensure maximum heat dissipation and to reduce thermal rise on the TSL8329-EVB-A during high power evaluations, this support plate must be attached to a heat sink using thermal grease.

Note that the measurements performed at the SMA connectors of the TSL8329-EVB-A include the losses of the SMA connectors and the PCB. The through line must be measured to calibrate out the TSL8329-EVB-A effects. The through line is the summation of an RF input line and an RF output line that are connected to the device and equal in length.

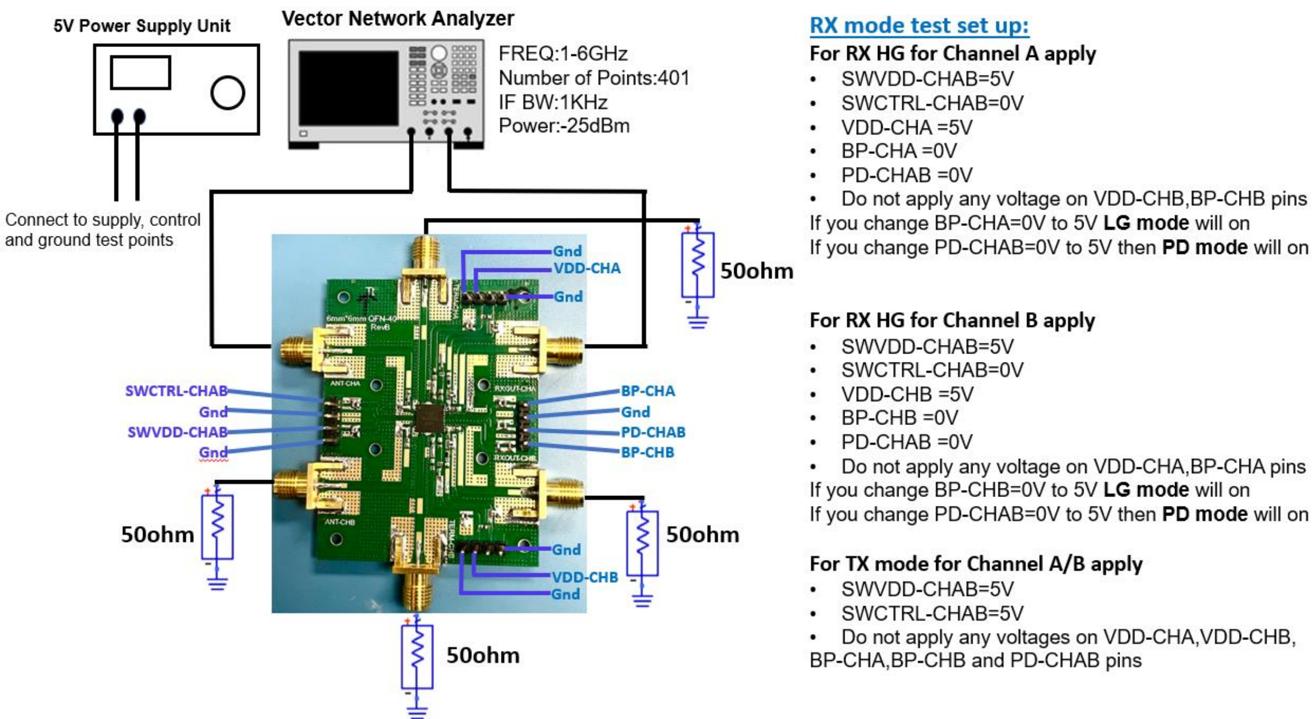


Figure 10.7.1 TEST Set Up Diagram for RX-mode

11.0 Device Package Information

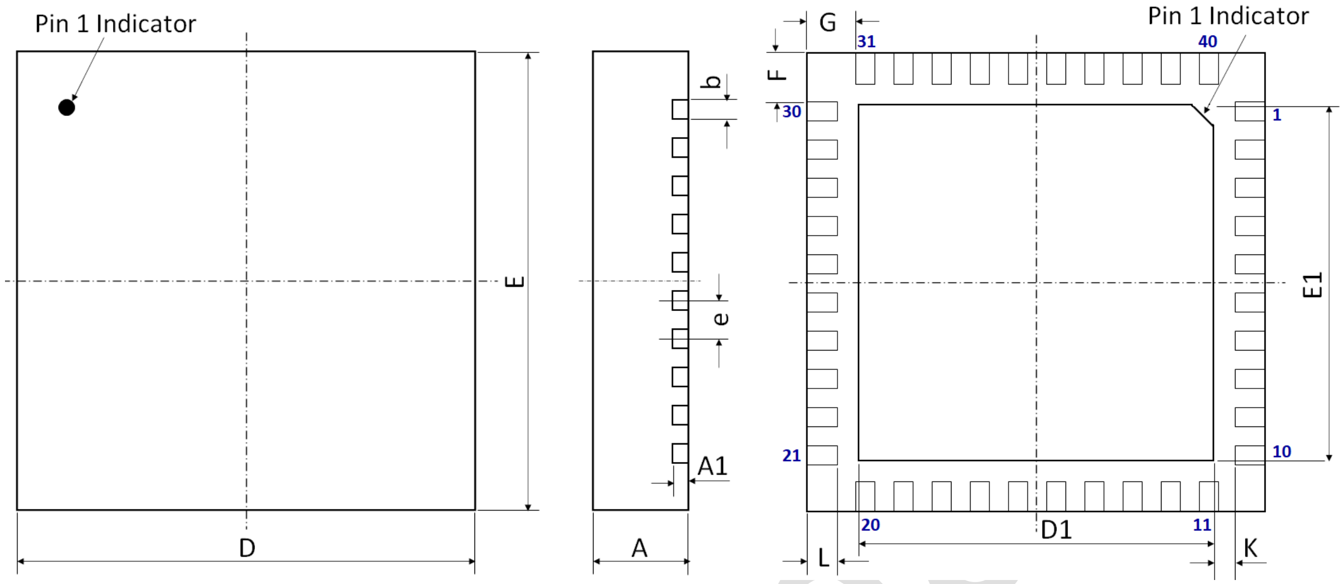


Figure 11.1 Device Package Drawing
(All dimensions are in mm)

Table 11.1 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.85	±0.05	E	6.00 BSC	±0.05
A1	0.203	±0.02	E1	4.65	±0.06
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	6.00 BSC	±0.05	G	0.625	±0.05
D1	4.65	±0.06	L	0.40	±0.05
e	0.50 BSC	±0.05	K	0.275	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5 µm ~ 20 µm (Typical 10 µm ~ 12 µm)

Attention:
Please refer to application notes *TN-001* and *TN-003* at http://www.tagoretech.com for PCB and soldering related guidelines.

12.0 PCB Land Design

Guidelines:
[1] 4-layer PCB is recommended.
[2] Via diameter is recommended to be 0.3 mm to prevent solder wicking inside the vias.
[3] Thermal vias shall be placed on the center pad and should be filled/plugged with solder or copper.
[4] The maximum via number for the center pad is 9(X)×9(Y)=81.

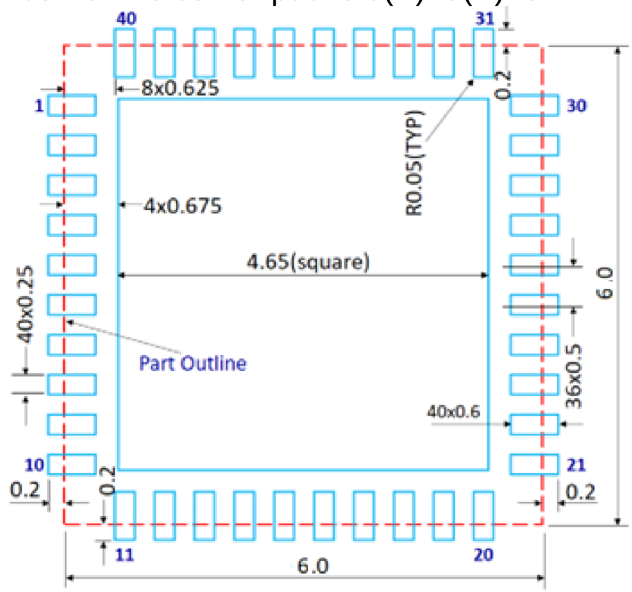
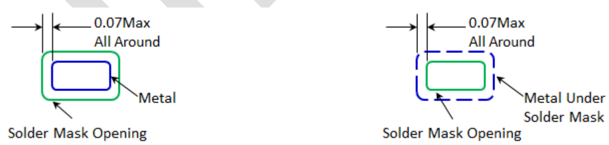


Figure 12.1 PCB Land Pattern
(Dimensions are in mm)



Non-Solder Mask Defined (Preferred) Solder Mask Defined

Figure 12.2 Solder Mask Pattern
(Dimensions are in mm)

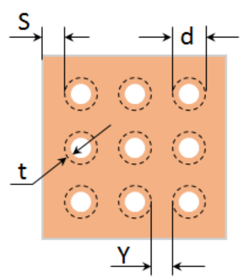


Figure 12.3 Thermal Via Pattern
(Recommended Values: S≥0.15 mm; Y≥0.20 mm; d=0.3 mm; Plating Thickness t=25 μm or 50 μm)

13.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125 μm.

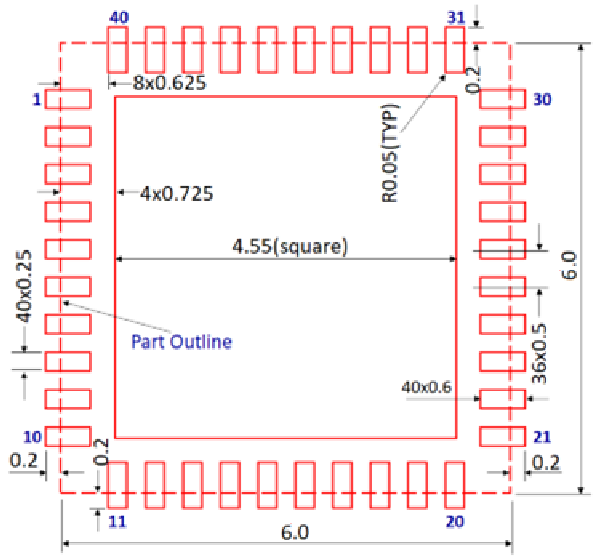


Figure 13.1 Stencil Openings
(Dimensions are in mm)

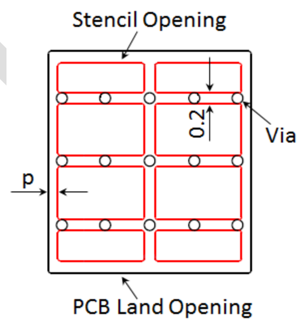


Figure 13.2 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

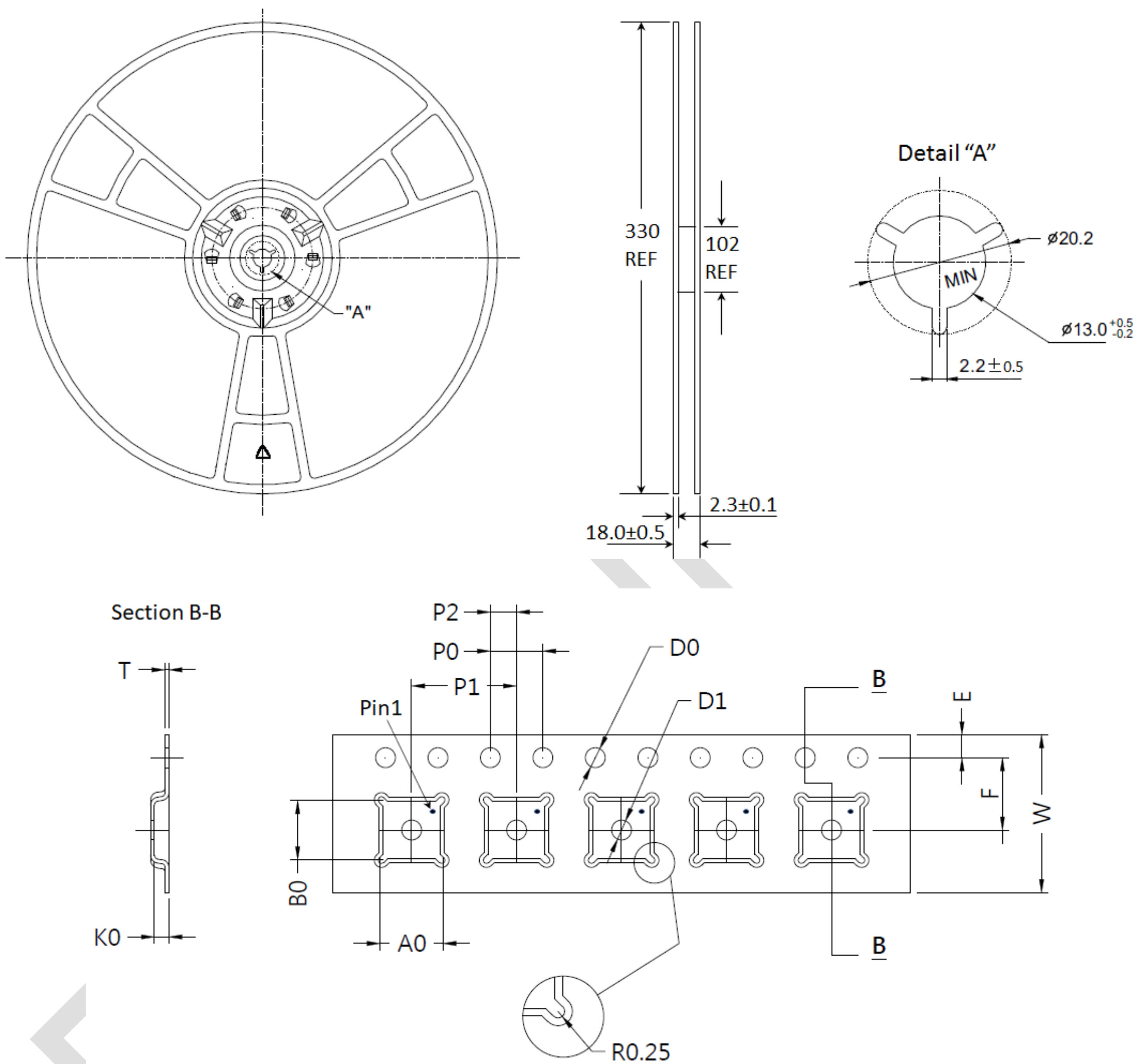


Figure 14.1 Tape and Reel Drawing

Table 14.1 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	6.35	±0.10	K0	1.10	±0.10
B0	6.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

Edition Revision 2.6 - 2024-07-30

Published by

TagoreTech Inc.

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Arlington Heights, IL 60004, USA

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