PCB DESIGN GUIDELINES FOR QFN PACKAGES

TN-001

01/22/2018

APPLICABLE TAGORE'S QFN PACKAGES

S/N	PACKAGE NO.	DESCRIPTION	NOTE
1	QFN-3X3-16-0.5	16 PIN 3x3mm QFN Pitch 0.5mm	**Pb-Free RoHS Compliance:** RoHS Directive 2011/65/EU – Annex II and Amending Directive 2015/863 **REACH Compliance:** REACH – Jan. 12, 2017 **Halogen Free Compliance:** IEC 61249-2-21:2003 Type: Molded or Air Cavity Pin Finish: Tin (Sn) MSL: 1
2	QFN-4X4-32-0.4	32 PIN 4x4mm QFN Pitch 0.4mm	
3	QFN-5X5-32-0.5	32 PIN 5x5mm QFN Pitch 0.5mm	
4	QFN-5X7-22-0.5	22 PIN 5x7mm QFN Pitch 0.5mm	
5	QFN-6X3-32-0.4	32 PIN 6x3mm QFN Pitch 0.4mm	
6	QFN-6X6-48-0.4	48 PIN 6x6mm QFN Pitch 0.4mm	
7	QFN-8X10-30-0.5	30 PIN 8x10mm QFN Pitch 0.5mm	
8	Other QFN Package Types Provided by Tagore		

1.0 Scope

The intent of this application note is to provide PCB designers with a set of guidelines for successful board mounting of Tagore's Quad Flat No-leads (QFN) packages. The QFN package is a near chip scale plastic encapsulated (molded) or air cavity package with a copper lead frame substrate, the electrical contact to PCB is made by soldering the lands on the bottom surface of the package to PCB, instead of the conventional formed perimeter leads. The exposed die attach pad(s) at the bottom of the package can effectively transfer heat to PCB and provide stable electrical connections if applicable.

2.0 Terms and Definitions

BSC	Basic Spacing between Centers, a term that appears on IC package drawings in reference to nominal dimensions.
GaN	Gallium Nitride
IEC	International Electrotechnical Commission
IPC	Institute for Printed Circuits
MSL	Moisture Sensitivity Level
NSMD	Non-Solder Mask Defined
Pb	Lead
PCB	Printed Circuit Board
PTH	Plated Through Hole
QFN	Quad Flat No-leads
REACH	Registration, Evaluation, Authorization and Restriction of Chemicals
RoHS	Restriction of Hazardous Substances
SMD	Solder Mask Defined
Sn	Tin

3.0 Disclaimer

This document only states general guidelines for PCB design using Tagore's semiconductor devices packed with QFN packages. Tagore does not make direct recommendations for PCB design nor does it take legal liability and responsibility for the information in this document. Please refer to the IPC website for more information regarding PCB design.

4.0 PCB Footprint Design Guidelines

For enhanced thermal, electrical, and board level performance, the exposed pads at the bottom of the QFN packages need to be soldered to PCB using surface mount process. Furthermore, for proper heat conduction through the PCB, thermal vias need to be incorporated in the PCB in thermal pad region. The PCB footprint design needs to consider dimensional tolerances related to package, PCB, and assembly factors.

Figure 4.1 to 4.4 show drawings of a typical QFN package and its corresponding PCB footprint, Table 4.1 summarize the recommended formulas and values to calculate dimensions in Y (vertical) direction for PCB footprint as well as thermal vias based on following design guidelines, the formulas and values are also applicable to dimensions in X (horizontal) direction.

(1) For good solder filleting, the PCB terminal pads should be 0.2mm to 0.5mm longer (away from package center) than the package terminal length (Y2 in Figure 4.2) and also should be extended 0.05mm toward the centerline of the package (Y1 in Figure 4.2).

(2) To minimize solder bridging, the pad width (H in Figure 4.3) should be the maximum width (b in Figure 4.1) of the component terminal for lead pitches below or equal to 0.65mm. If the pitch is more than 0.65mm, the pad width H can be 0.1mm wider than b (add 0.05mm on each of the two sides).
(3) To prevent solder bridging, the clearance (P in Figures 4.2 and 4.3) between terminal pads and center pad(s) shall be 0.15mm minimum, recommend 0.2mm.
(4) The minimum drilling diameter of the vias (Vd in Figure 4.4) is 0.2mm, the diameter can be 0.2mm, 0.25mm, 0.3mm, 0.33mm, etc., recommend 0.3mm.
(5) The minimum distance between the drilling edges of vias (V2 in Figure 4.4) is 0.2mm.
(6) The minimum distance between the drilling edge of a via and the edge of the thermal pad (V1 in Figure 4.4) can be 0.1mm, but recommend 0.2mm.
(7) The plating thickness (copper) of the vias (Vt) is 0.025mm (1mil) typical, can increase to 0.050mm (2mils).
(8) The terminal pads can be larger than those shown in the Figures, the guidelines are also valid to the larger terminal pads, and vias can be designed on bigger terminal pads as well.
(9) For vias with drilling diameters less than or equal to 0.3mm, it is normally not necessary to cover the vias with solder mask, since solder mask may cause excessive solder voiding.
(10) If the via drilling diameters are more than 0.3mm, solder masking may be required to prevent solder wicking inside the vias during reflow, the methods include via tenting (from top or bottom) using dry film solder mask, via plugging (completely or partially) with conductive or non-conductive via fill materials, etc., depending on power level and/or application. These methods will of course increase PCB cost.

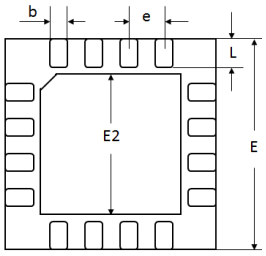

Figure 4.1
QFN Footprint
(Top View)

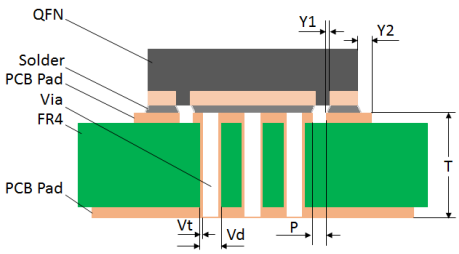

Figure 4.2
Cross Section of QFN-PCB

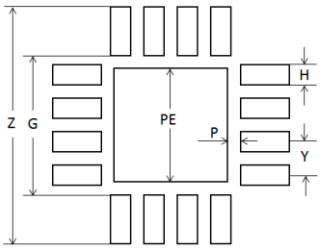

Figure 4.3
PCB Footprint
(Top View)

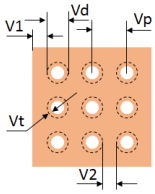

Figure 4.4
Vias on Big Pad (Top View)

TABLE 4.1 Recommended Calculation Formulas and Values

S/N	Dimension	**Minimum** (mm)	**Recommend** (mm)	**Maximum** (mm)
1	G	E(BSC) - 2×L(max) - 2×Y1	-	-
2	H	-	b(max) ~ if pitch ≤0.65	b(max)+0.1 ~ if pitch >0.65
3	P	0.15	0.20	-
4	PE	-	-	G - 0.4
5	V1	0.15 (Recommend 0.20)	-	-
6	V2	0.20	-	-
7	Vd	0.20	0.30	-
8	Vt	-	0.025	0.050
9	Y	-	e(BSC)	-
10	Y1	-	0.05	-
11	Y2	0.20	-	0.50
12	Z	E(BSC) + 0.55	-	E(BSC) + 1.15

5.0 Solder Mask Design Guidelines

(1) The clearance (Sc in Figure 5.1) between copper pad and the solder mask shall be 0.015mm to 0.020mm. Typically each pad can have its own solder mask opening for a lead pitch of 0.5mm or higher (Figure 5.1). However, it is recommended to use solder mask opening as shown in Figure 5.2 for finer pitch devices. The inner edges of the solder mask should be rounded.
(2) It is recommended that the thermal pad area should be solder mask defined to avoid any solder bridging between the thermal pad and the perimeter pads. The mask opening should be 0.025mm smaller than the thermal land size on all four sides.

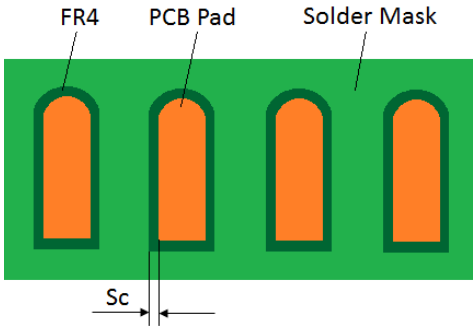

Figure 5.1 Solder Mask for ≥0.5mm Pitch Pins

Figure 5.2 Solder Mask for <0.5mm Pitch Pins

6.0 Stencil Design Guidelines

(1) A stencil thickness of 0.125 mm is recommended for devices with ≤0.5mm pitch. The thickness can be 0.15mm to 0.20mm for parts with >0.5mm pitch.
(2) Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
(3) To maximize solder paste release, the stencil aperture opening should be designed to meet following requirements:

Area Ratio = Area of Aperture Opening / Aperture Wall Area ≥ 0.66
Aspect Ratio = Aperture width / Stencil Thickness ≥ 1.5

For rectangular aperture openings, these ratios are given as:

Area Ratio = LW / 2T(L+W)
Aspect Ratio = W / T

Where L and W are the aperture length and width, and T is stencil thickness.

(4) The stencil aperture should be 1:1 to the PCB pad size or area need to be soldered.
(5) It is recommended that smaller multiple openings as shown in Figures 6.1 and 6.2 in the stencil should be used instead of one big opening for printing the solder paste if the soldered area is too large (such as ≥7mmx7mm), but the solder paste coverage shall be 50% minimum of the openings for plugged vias, and 75% minimum for non-plugged vias.

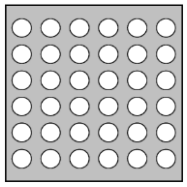

Figure 6.1 Circle Pattern

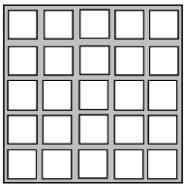

Figure 6.2 Rectangular Pattern